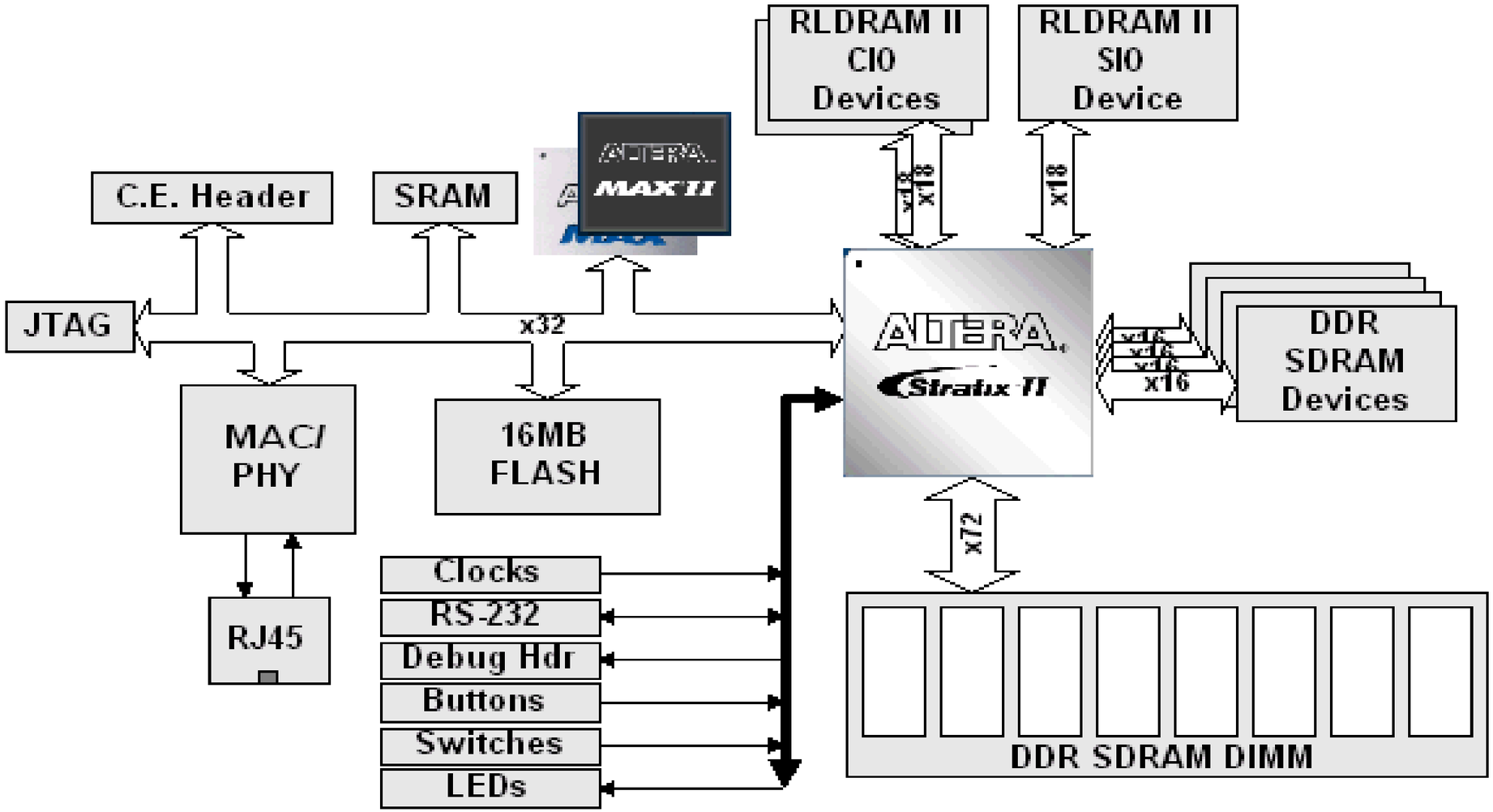
NOTES:

1. Altera Stratix Schematic Symbol Breakdown:
   - (a) Bank1 - DDR SDRAM DEVICES
   - (b) Bank2 - DDR SDRAM DEVICES
   - (c) Bank3 - RLDRAM II SIO DEVICE
   - (d) Bank4 - RLDRAM II CIO DEVICES
   - (e) Bank5 - GENERAL PURPOSE I/O
   - (f) Bank6 - GENERAL PURPOSE I/O
   - (g) Bank7 - DDR SDRAM DIMM
   - (h) Bank8 - DDR SDRAM DIMM
   - (i) Configuration/GPIO
   - (j) Clocks/GPIO
   - (k) VCCINT/GND
   - (l) VCCIO/GND

Stratix II Memory Board 1 Block Diagram



REV	DATE	PAGES	DESCRIPTION
A	10/18/2004	all	Design Release

PAGE	DESCRIPTION
1	TITLE, NOTES, REVISION HISTORY
2	STRATIX II PACKAGE LAYOUT
3	POWER SUPPLY 1
4	POWER SUPPLY 2
5	STRATIX II PLL AND POWER
6	STRATIX II VTC SENSE
7	CLOCK CIRCUITRY
8	MAX CONFIGURATION
9	MAX II CONFIGURATION 256 FBGA
10	STRATIX II BANK 3, 4
11	RLDRAM II SIO
12	RLDRAM II SIO TERMINATIONS
13	RLDRAM II CIO 1
14	RLDRAM II CIO 1 TERMINATIONS
15	RLDRAM II CIO 2
16	RLDRAM II CIO 2 TERMINATIONS
17	STRATIX II BANK 1, 2
18	DDR SDRAM PAGE 1
19	DDR SDRAM TERM PAGE 1 (SHARED)
20	DDR SDRAM A AND B TERMINATIONS
21	DDR SDRAM PAGE 2
22	DDR SDRAM C AND D TERMINATIONS
23	STRATIX II BANK 7, 8
24	DDR SDRAM DIMM
25	DDR SDRAM DIMM TERM PAGE 1
26	DDR SDRAM DIMM TERM PAGE 2
27	STRATIX II BANK 5, 6
28	SRAM and FLASH
29	10/100 ETHERNET
30	RS-232
31	DEBUG PROTO HEADERS
32	SEVEN SEGMENT DISPLAYS AND LEDS
33	PUSH BUTTONS / DIP SWITCHES
34	STRATIX II DECOUPLING CAPS
35	MAX II SSO, TQ144

PLL Ground

Ground

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Stratix II Memory Board IO Bank Diagram

Stratix II F1020 Package Top View

BANK 4

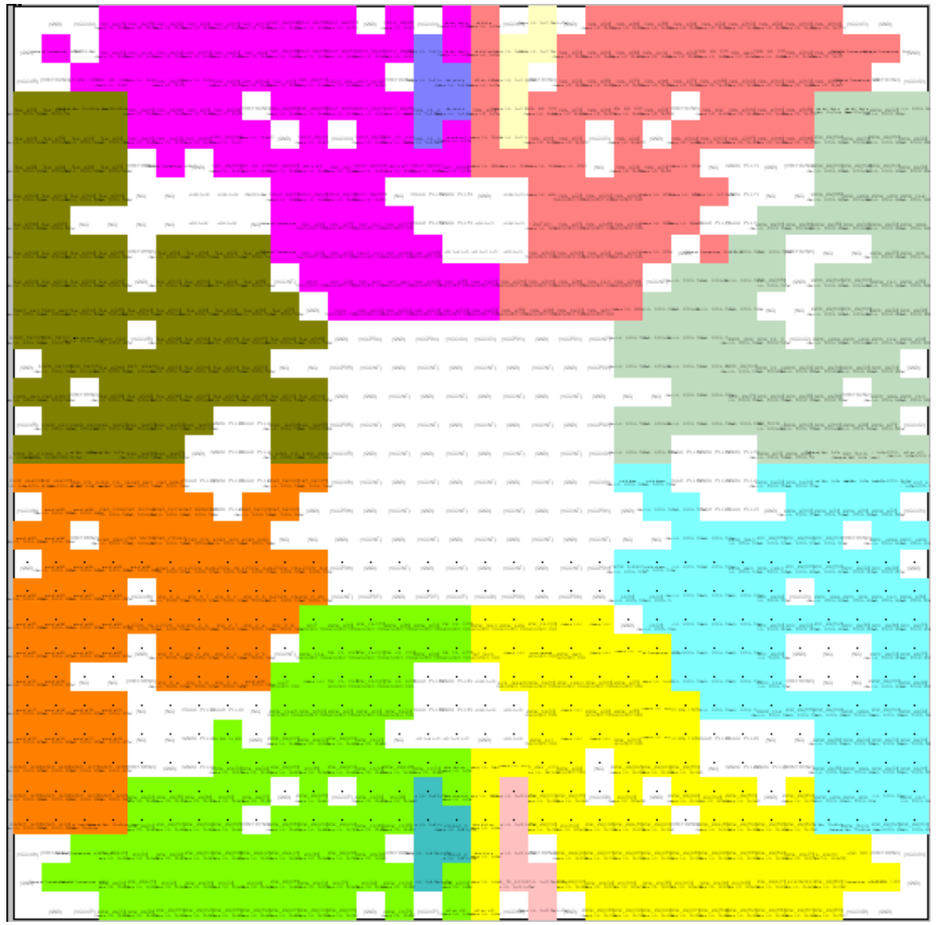
VCCIO = 1.5V / 1.8V

RLDRAM II CIO DEVICES

BANK 3

VCCIO = 1.5V / 1.8V

RLDRAM II SIO DEVICE



BANK 5

VCCIO = 3.3V

x32 SHARED DATA BUS
x26 SHARED ADDRESS BUS
FLASH SIGNALS
SRAM SIGNALS
USER LEDs

BANK 2

VCCIO = 2.6V

DDR SDRAM DEVICES

BANK 6

VCCIO = 3.3V

PUSH BUTTON INPUTS
ETHERNET SIGNALS
DEBUG PORT SIGNALS
RS-232 SIGNALS
7-SEGMENT DISPLAYS

BANK 1

VCCIO = 2.6V

DDR SDRAM DEVICES

BANK 7

VCCIO = 2.6V

DDR DIMM
DIPSWITCH

BANK 8

VCCIO = 2.6V

DDR DIMM
DIPSWITCH

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Power Supply 1 of 2

9V - 20V
DC Input

(Board Max 60W)

J1
CONN JACK PWR

C4 47uF
C47 10uF
C49 10uF
C56 10uF
C51 10uF
C52 10uF
C60 10uF

Q4 Si4856DY
Q1 Si4856DY
Q7 Si4856DY
Q2 Si4856DY
Q5 Si4856DY
Q6 Si4856DY

PWR_IN
1.2V_TGATE
3.3V_TGATE
1.2V_SWITCH
3.3V_SWITCH
INTVCC

L4 1.0uH
L5 1.0uH

6 1.2V_INT_SENSE_P
6 1.2V_INT_SENSE_N

Place 0 Ohm resistors as close as possible to the 0.003 resistor

D6 MBRS130L
D12 MBRS130L
D7 MBRS130L
D9 CMDSH2-3
D10 CMDSH2-3

C57 0.1uF
C58 0.1uF
C67 10uF

R22 0
R20 0
R15 0
R16 0
R28 0
R23 0
R3 0.003
R4 0.003

1.2V_INDOUT
1.2V_BGATE
1.2V_BOOST
1.2V_SW
1.2V_SENSE_P1
1.2V_VOSENSE
1.2V_ITH

U17
LTC3728
Vin
INTVcc
EXTVcc
TG1
BOOST1
SW1
BG1
SENSE1+
SENSE1-
Vosense1
Ith1
RUN/SS1
FCB
PGOOD
TG2
BOOST2
SW2
BG2
SENSE2+
SENSE2-
Vosence2
Ith2
RUN/SS2
3.3Vout
PLLFLTR
SGND
PLLIN
PGND

3.3V_BOOST
3.3V_SW
3.3V_BGATE
3.3V_SENSE_P
3.3V_SENSE_N
3.3V_VOSENSE
3.3V_ITH

C74 0.001uF
C69 0.001uF

Place 0 Ohm resistors as close as possible to the 0.003 resistor

J2
BANANA JACK
+1.2V @ 15A

1.2V_INT

F1 15.0A
F2 7.0A

R36 510
R35 6.34K

C1 10uF
C2 10uF
C11 180uF
C12 180uF
C6 10uF
C5 10uF
C35 180uF
C31 180uF
C71 680pF
C70 33pF
C68 0.1uF
C59 0.1uF
C72 33pF
C73 680pF
C13 180uF
C7 10uF
C8 180uF

R34 1.00K
R37 10K
R38 10K
R39 2.00K

J3
BANANA JACK
+3.3V @ 7A

3.3V_SENSE_P1 6
3.3V_SENSE_N1 6
3.3V_SENSE 6
3.3V
R5 0.01
C32 10uF
C33 10uF

1.2V_SHDN
3.3V_SHDN
SW1
SW SLIDE-4P2T

PWR_IN
R1 1K
D1 LED
A
C
BLUE
PWR_ON_LED_RES
PWR_ON_LED

J5
BANANA JACK
J21
BANANA JACK

Main Power Switch

J18
BANANA JACK
1.5V/1.8V @ 1.5A

3.3V
R297 0.033 1W
R287 1K
RLD_PWR
VCCIO_RLD_REG_IN
C287 10uF
U39
EN OUT
IN
GND
TAB ADJ
MIC29502BU
HS3
HS1
7106D
RLDRAMIO_POUT
VCCIO_RLD_SEL
R290 10.2
C65 10uF
C66 47uF 6.3V Tantalum
F12 7.0A
C61 10uF
C63 100uF 10V Tantalum
VCCIO_RLD

RLD_PWR RLD_PWR 4,33
VCCIO_RLD_SEL VCCIO_RLD_SEL 33
1.2V_SHDN 1.2V_SHDN 33
3.3V_SHDN 3.3V_SHDN 33

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Power Supply 2 of 2

ADD GND TESTPOINTS ON
TOP AND BOTTOM OF BOARD
FOR PROBING.

RLD_PWR — RLD_PWR 3,33

VCCIO_ENABLE — VCCIO_ENABLE 8,9,33

J10 Banana jack — VREF_DDR — F8 7.0A — VTT_OUT_DDR / VREF_OUT_DDR

U3 LP2996MR: GND, SD, VSNS, VREF, GND1, VTT, PVIN, AVIN, VDDQ

3.3V — C28 0.1uF — C9 0.1uF

VTT_OUT_DDR — F9 7.0A — J11 Banana jack — VTT_DDR_SENSE 6

R2 0.01 — C3 0.1uF — C29 100uF 10V Tantalum — C30 100uF 10V Tantalum — VTT_DDR

2.6V_TERM — C34 0.1uF — C10 220uF 6.3V Tantalum — C36 100uF 10V Tantalum

L11 3.0A/50 — L15 3.0A/50 — L7 3.0A/50 — L17 3.0A/50 — L9 3.0A/50

TP1 TP4 TP7 TP15 TP13 — TP5 TP3 TP6 TP9 TP10 TP16 TP18 TP20 TP19 TP17

FAN_CNTL — J51 CON2

12V — J50 22_23_2021 — FAN_CNTL

6,23 S_OVERTEMPn — S_OVERTEMPn — Q8 FDV305N

J13 Banana jack — VREF_RLD — F10 7.0A — VTT_OUT_RLD / VREF_OUT_RLD

U10 LP2996MR: GND, SD, VSNS, VREF, GND1, VTT, PVIN, AVIN, VDDQ

3.3V — C43 0.1uF — C48 0.1uF

VTT_OUT_RLD — F11 7.0A — J16 Banana jack — VTT_RLD_SENSE 6

R13 0.01 — C46 0.1uF — C45 100uF 10V Tantalum — C44 100uF 10V Tantalum — VTT_RLD

VCCIO_RLD — C50 0.1uF — C54 100uF 10V Tantalum — C55 220uF 6.3V Tantalum

C40 10uF — C41 220pF — R11 10K — R9 1.1M — R8 78.7K

U4 LTC1872B: RUN, GND, VFB, VIN, SENSE-, NGATE

R7 0.033 — L3 10uH — D8 MBRS340 — Q3 FDS6612A — C53 47uF

J7 Banana jack — F5 7.0A — VCC_STXII_IO — L1 3.0A/50 — C20 10uF — C21 100uF 10V Tantalum — VCCIO_DDR

J9 Banana jack — F7 7.0A — 2.6V_MEM_TERM — L2 3.0A/50 — C27 47uF 6.3V Tantalum — C26 100uF 10V Tantalum — 2.6V_TERM

3.3V — R266 0.033 1W — R270 1K VCCIO_ENABLE — VCCIO_REG_IN — C255 10uF

U37 MIC29502BU: EN, OUT, IN, GND, TAB, ADJ

VCCIO_OUT — R268 102 — R276 93.1 — C254 10uF — C22 47uF 6.3V Tantalum

HS1 7106D

J20 Banana jack — 3.3V — R12 0.033 — C39 10uF

U12 MIC49300: EN, OUT, VBIAS, IN, GND, TAB

1.2V_OUT — C42 10uF — C23 47uF 6.3V Tantalum — F6 7.0A — J8 BANANA JACK RED — 1.2V_PLL — C25 10uF — C24 100uF 10V Tantalum

3.3V — R267 0.033 1W — R272 1K RLD_PWR — 1.8V_REG_IN — C257 10uF

U38 MIC29502BU: EN, OUT, IN, GND, TAB, ADJ

1.8V_OUT — R269 102 — R271 226 — C256 10uF — C16 47uF 6.3V Tantalum — F3 7.0A — J4 Banana jack — C15 10uF — C14 100uF 10V Tantalum — 1.8V

HS2 7106D

3.3V — R6 0.033 1W — RLD_PWR — 2.5V_REG_IN — C38 10uF

U11 MIC29502BU: EN, OUT, IN, GND, TAB, ADJ

2.5V_OUT — R10 104 — R14 102 — C37 10uF — C17 47uF 6.3V Tantalum — F4 7.0A — J6 Banana jack — 2.5V — C19 10uF — C18 100uF 10V Tantalum

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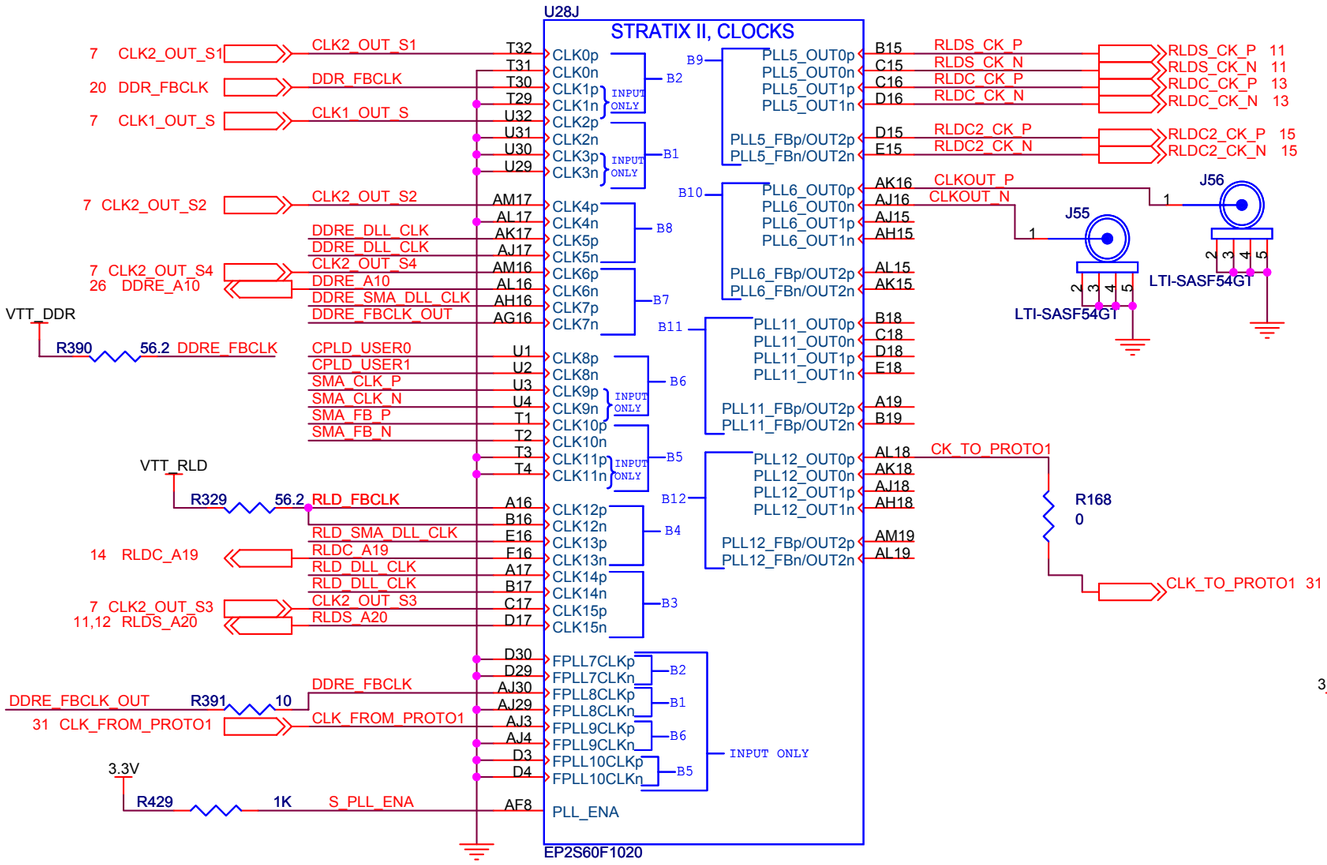
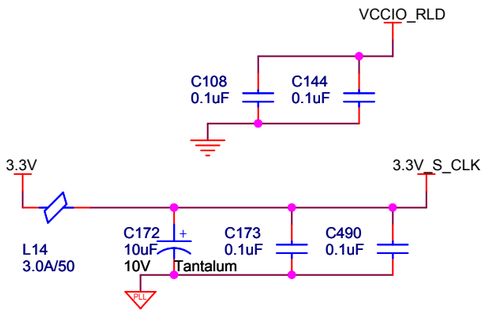
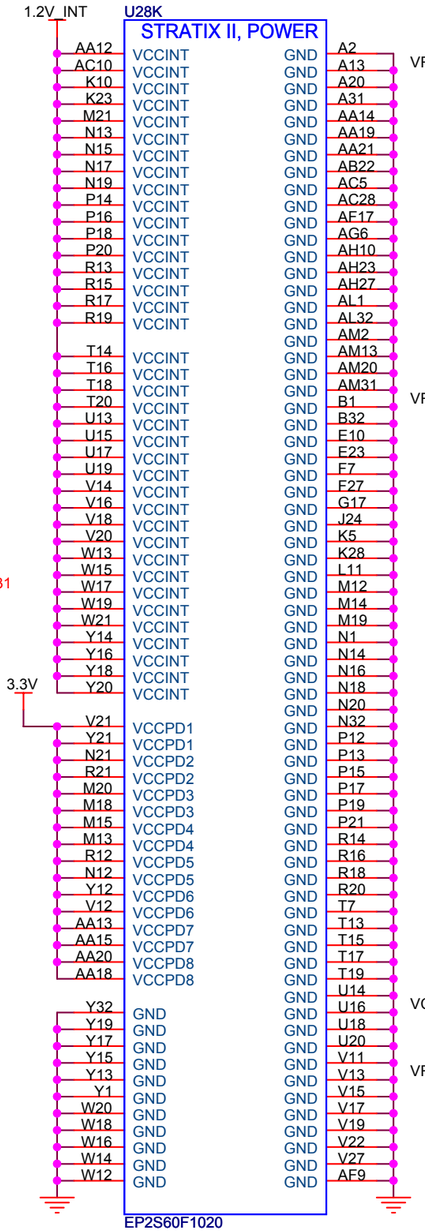
Stratix II PLL & Power

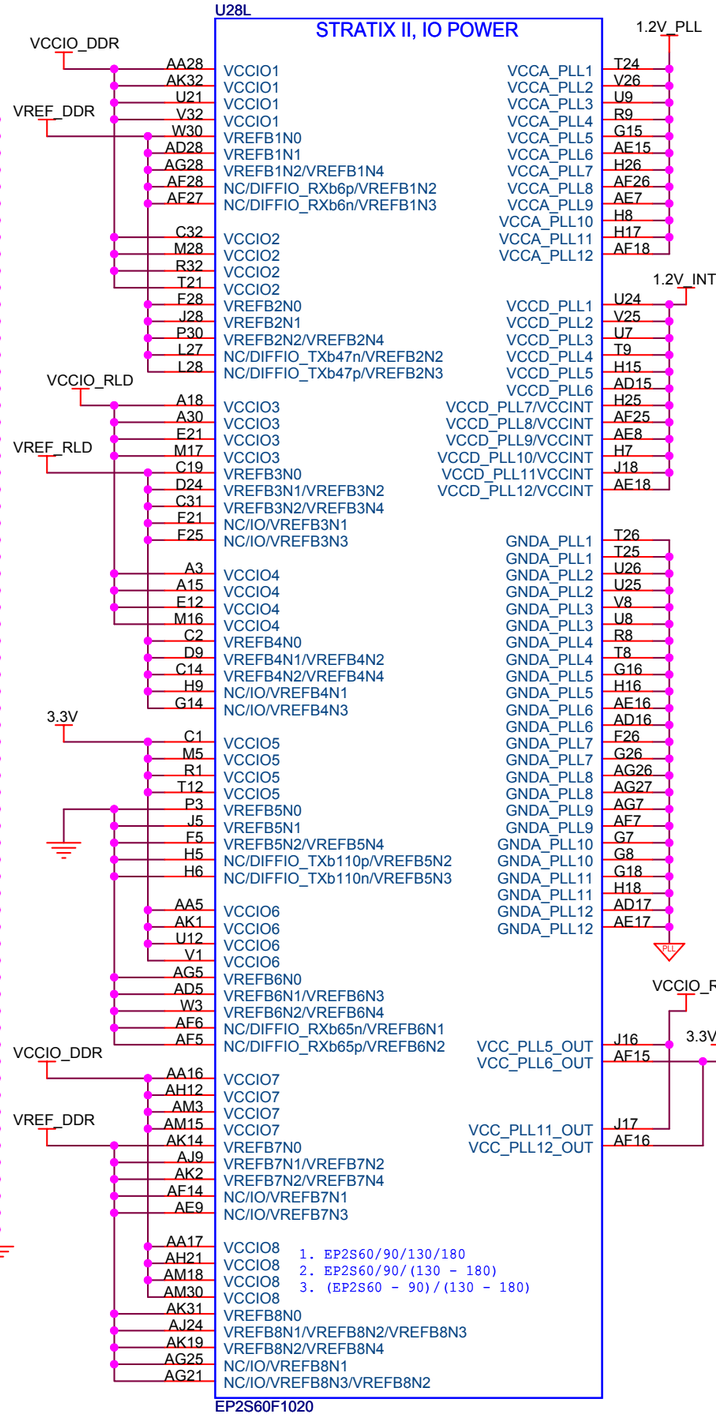




CPLD INTERFACE

CPLD_USER[1..0] — CPLD_USER[1..0] 8,9





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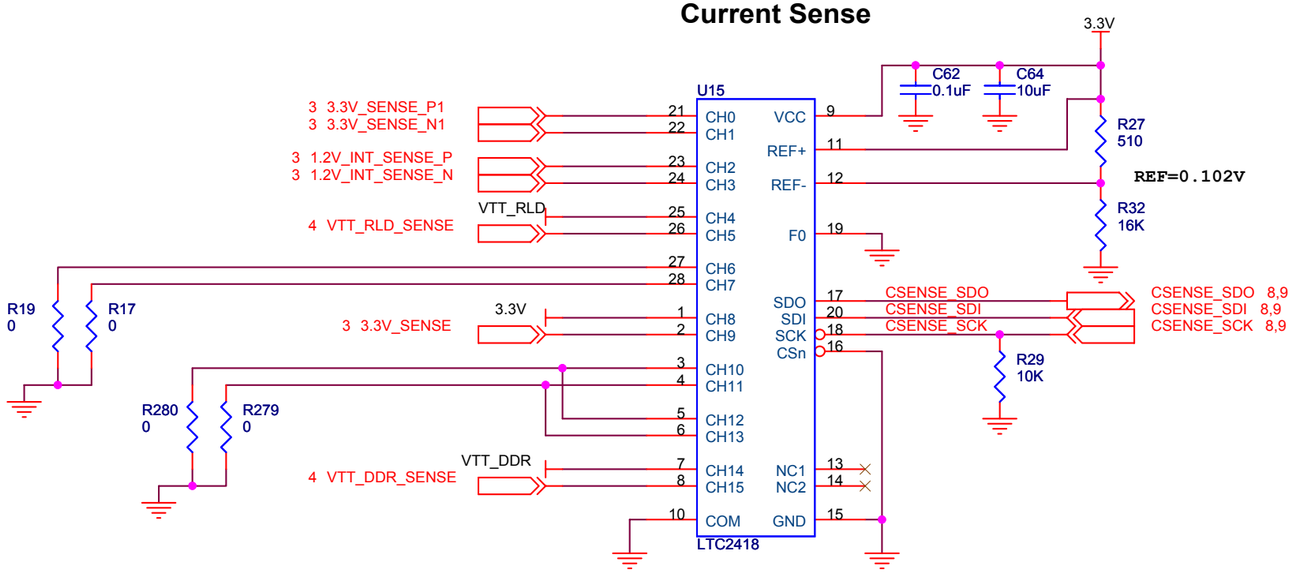
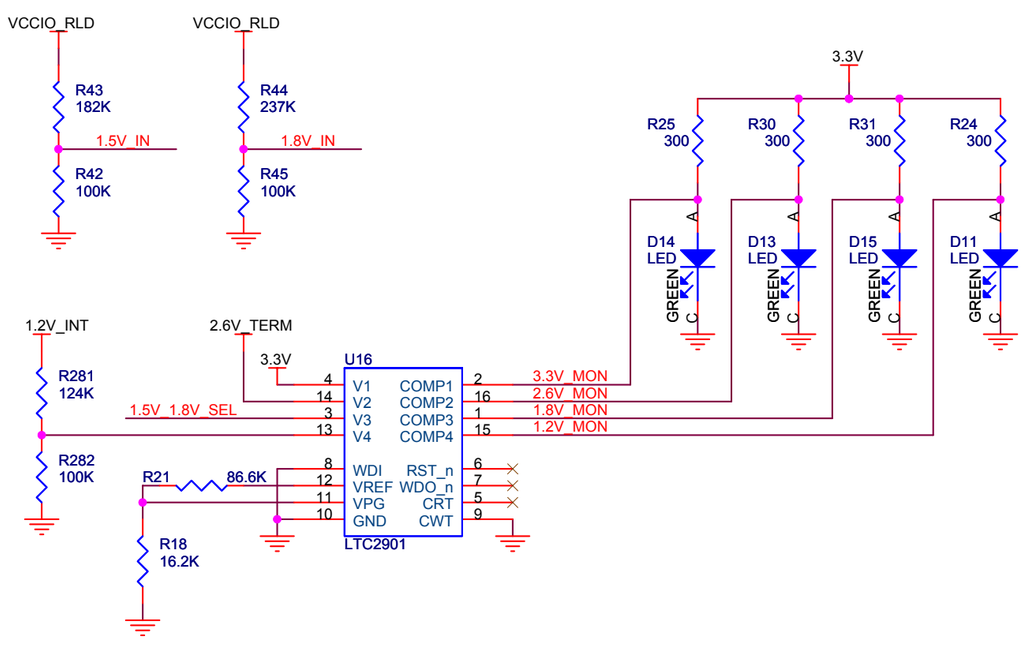
Stratix II Voltage, Temperature, & Current Sense

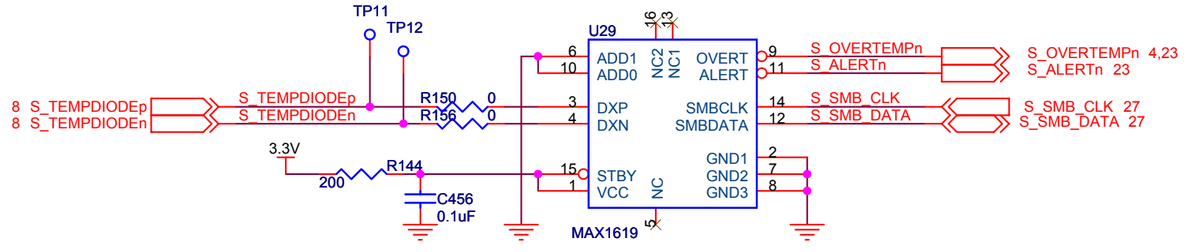
Current Sense

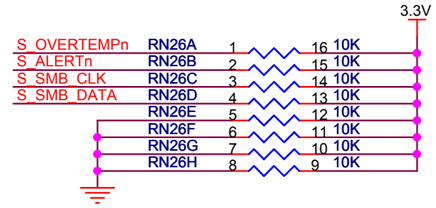


Voltage Sense



Temperature Sense





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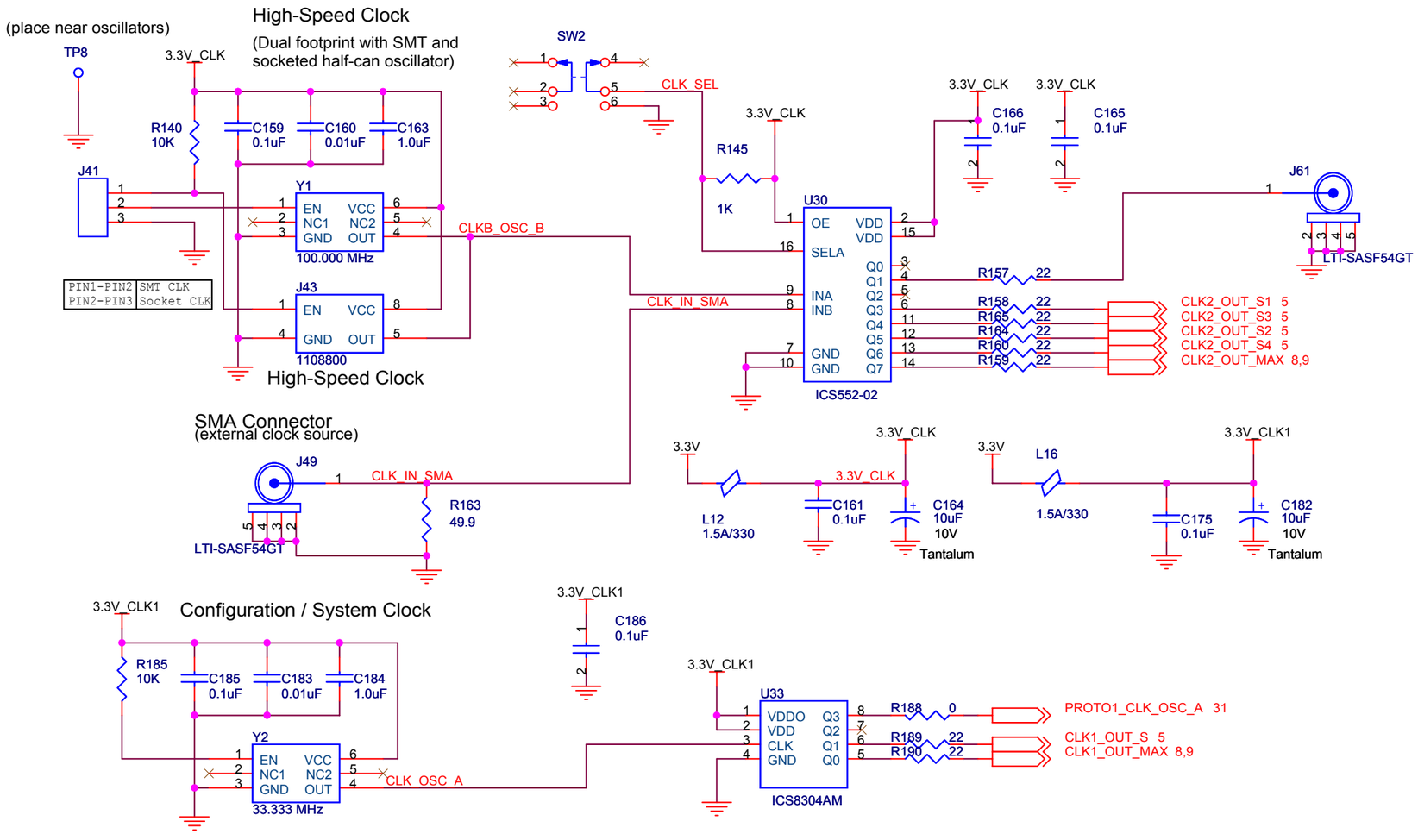
Clock Circuitry



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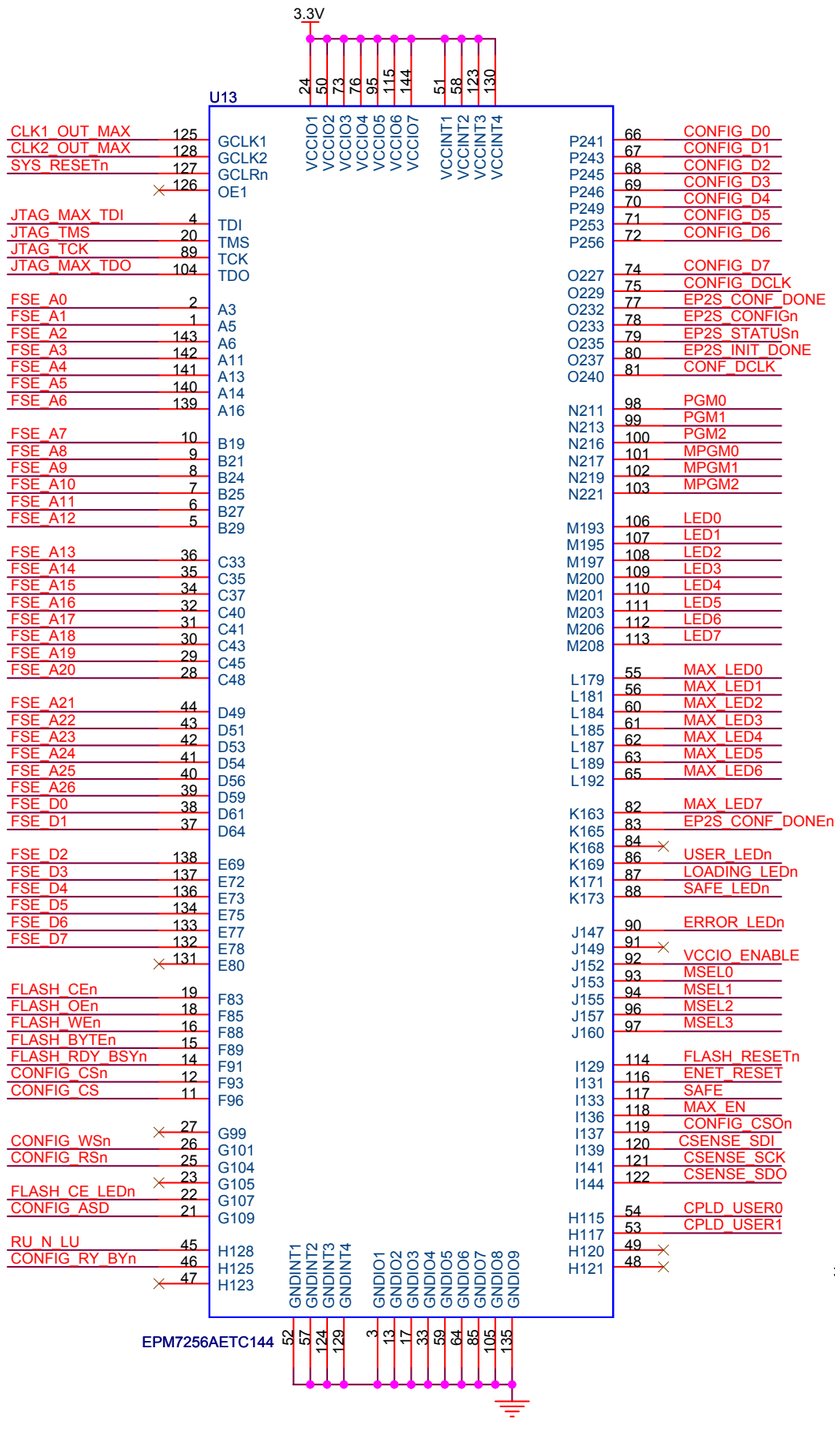
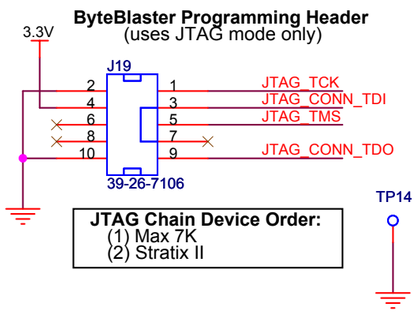
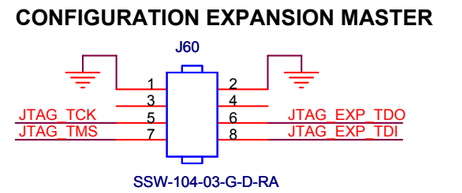
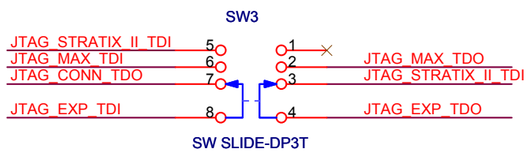
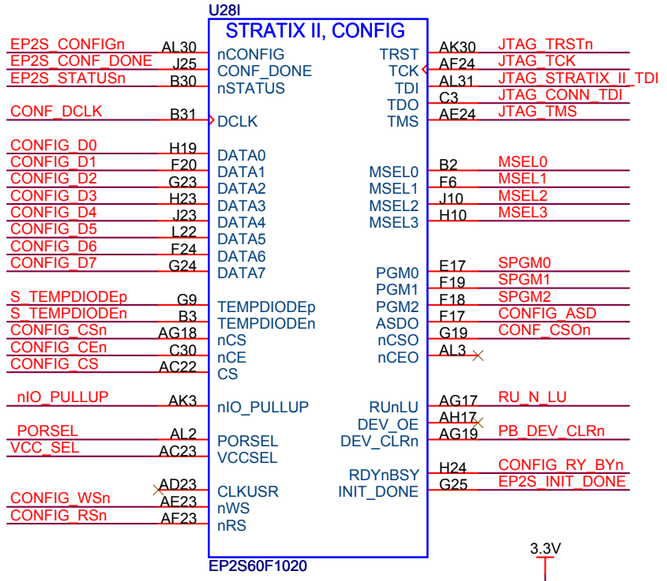
Max Configuration

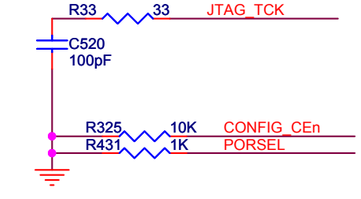


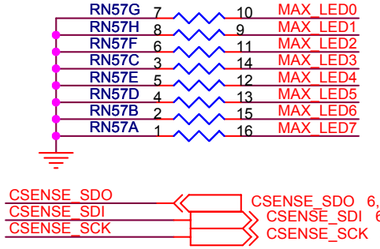


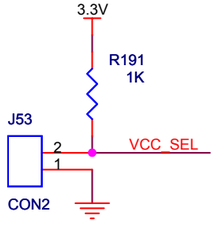


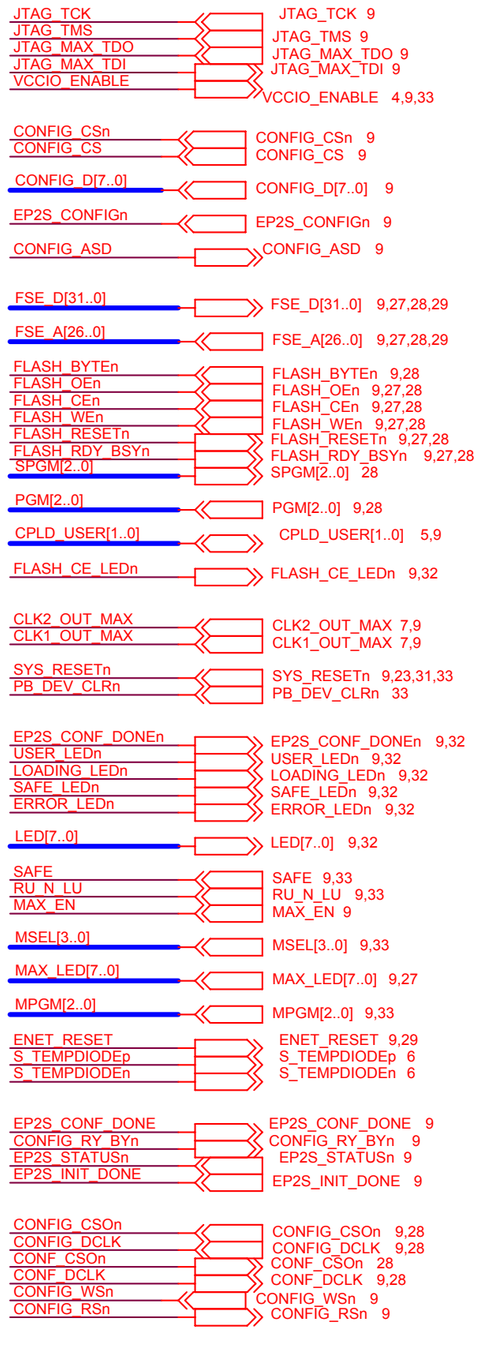












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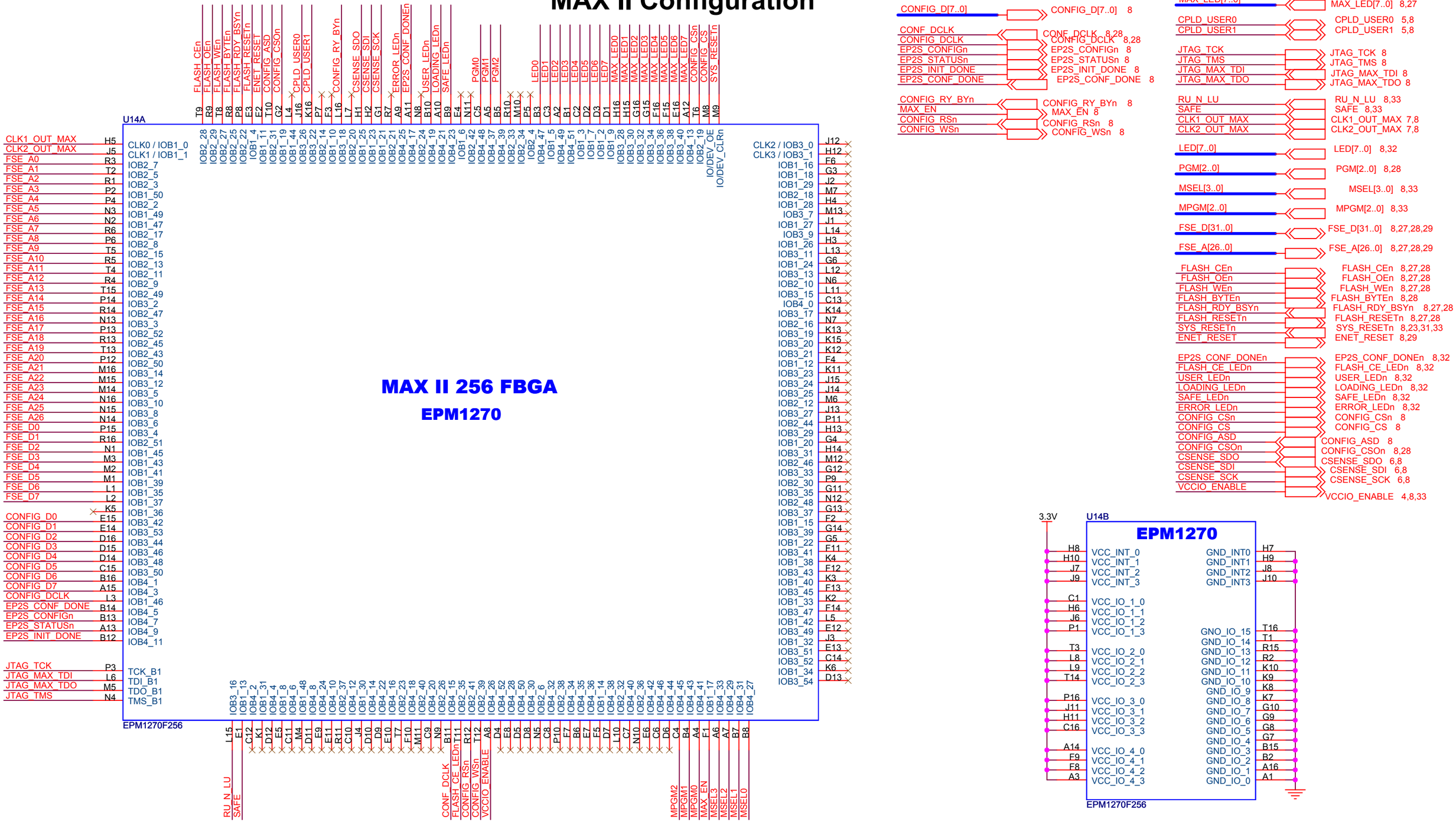
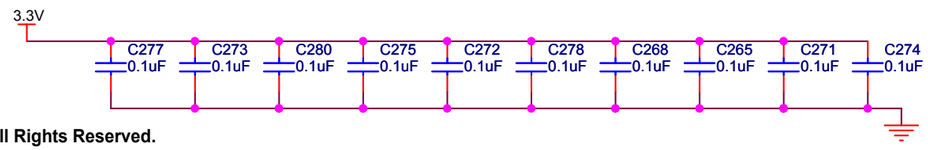
MAX II Configuration





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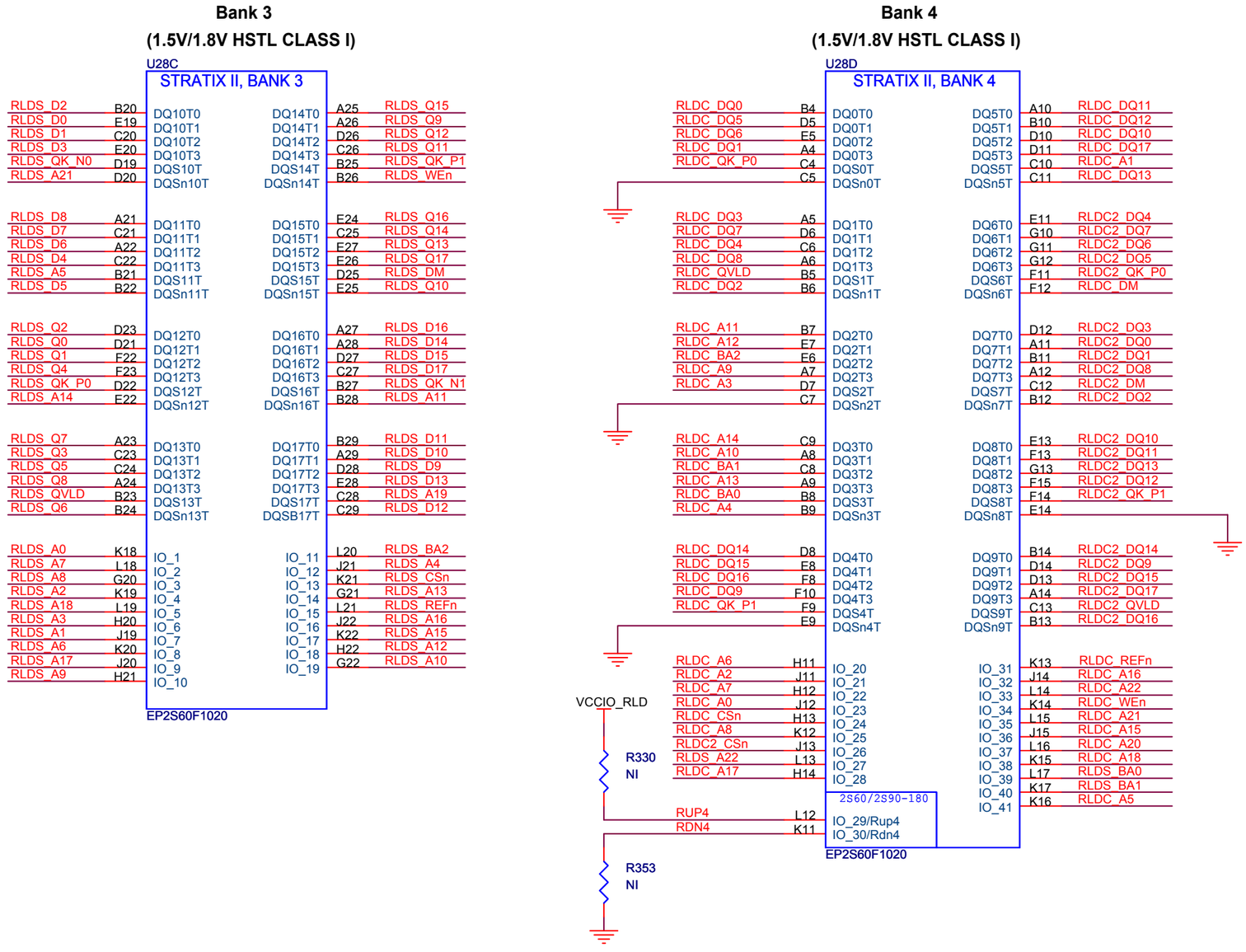
Stratix II Bank 3, Bank 4



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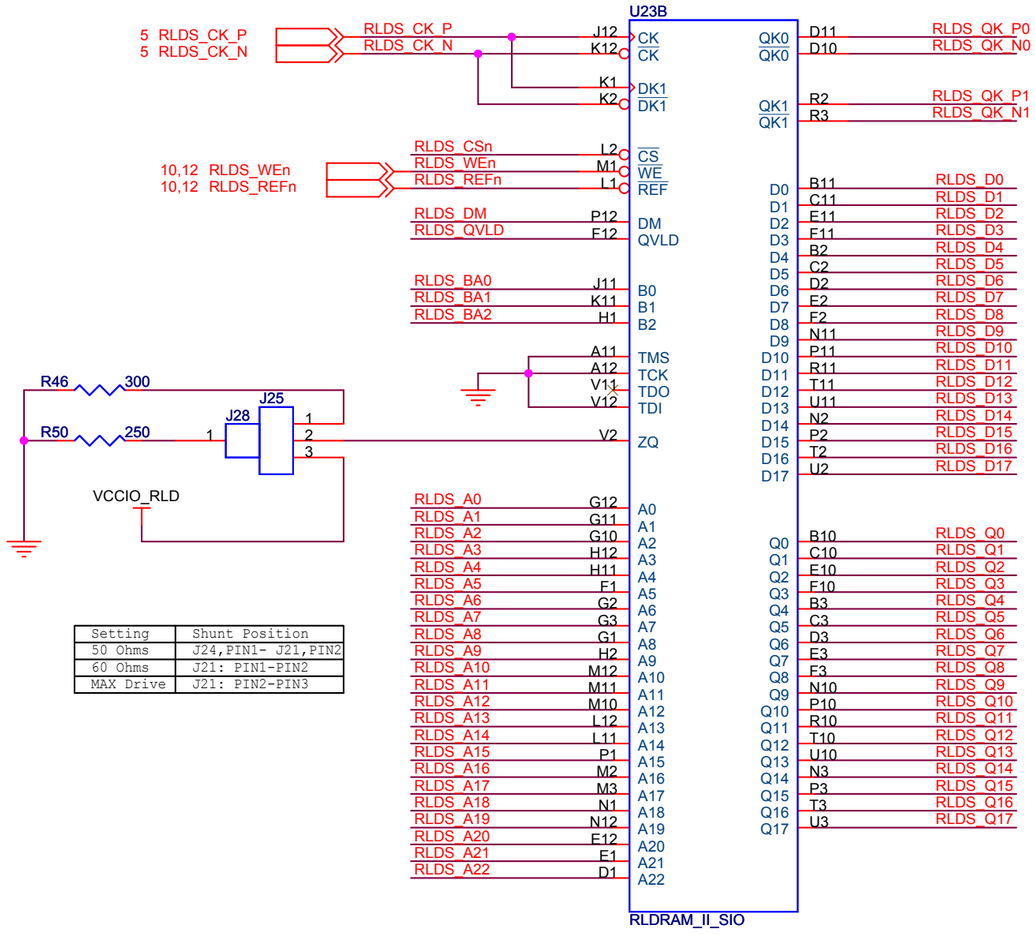
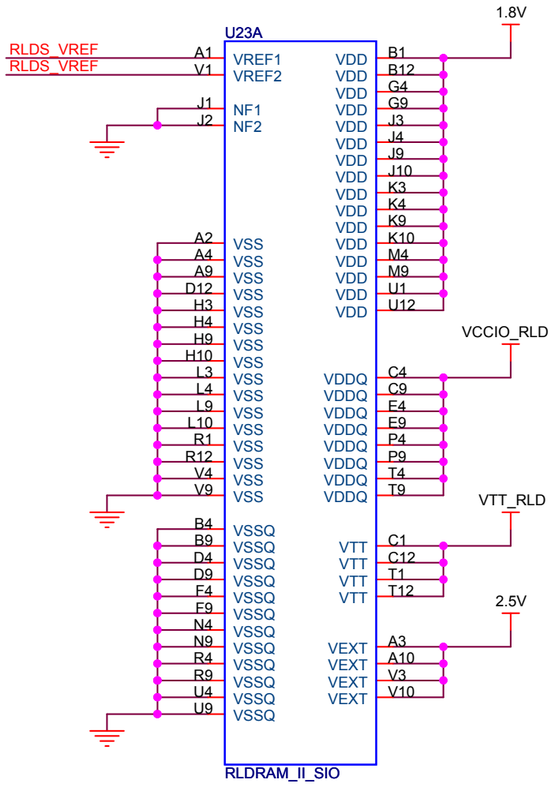
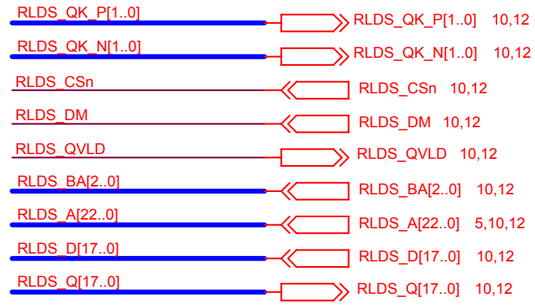
RLDRAM II SIO

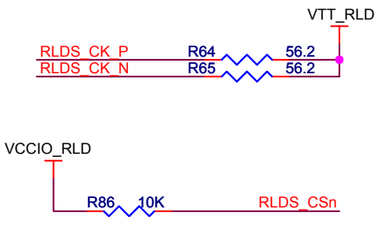


Setting	Shunt Position
50 Ohms	J24,PIN1- J21,PIN2
60 Ohms	J21: PIN1-PIN2
MAX Drive	J21: PIN2-PIN3

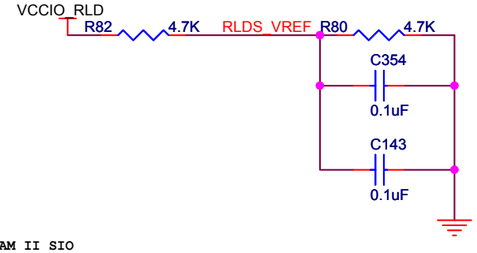




PLACE THESE RESISTORS AS CLOSE AS POSSIBLE TO THE RLDRAM

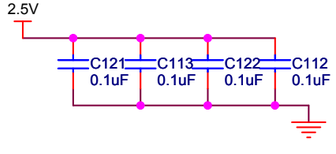


PLACE THESE RESISTORS AS CLOSE AS POSSIBLE TO THE RLDRAM

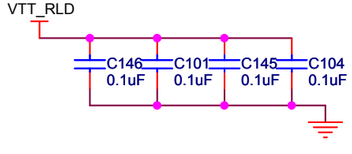


HSTL1

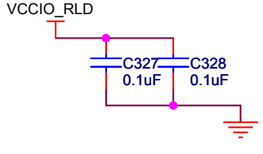
BYPASS CAPS FOR RLDRAM II SIO



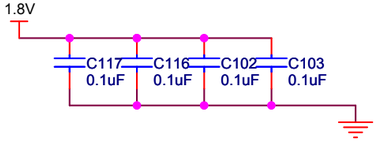
BYPASS CAPS FOR RLDRAM II SIO



BYPASS CAPS FOR RLDRAM II SIO



BYPASS CAPS FOR RLDRAM II SIO



Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title: **Stratix II Memory Board I**

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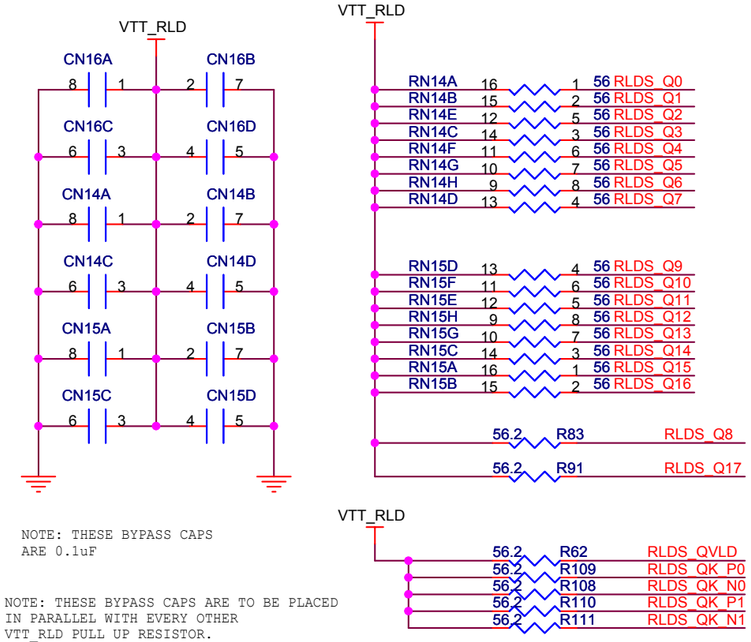
RLDRAM II SIO Terminations

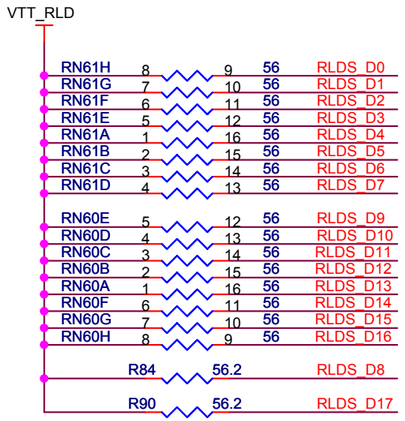
PLACE THE RESISTORS WITHIN THIS BOX AS CLOSE AS POSSIBLE TO THE STRATIX II DEVICE

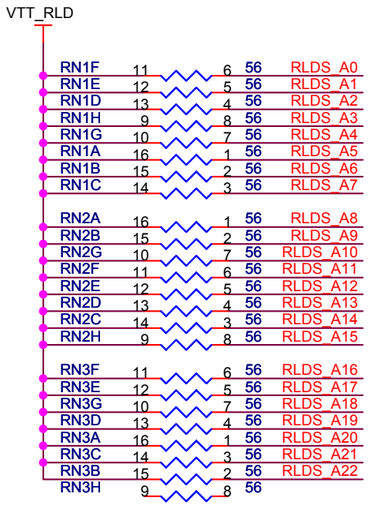


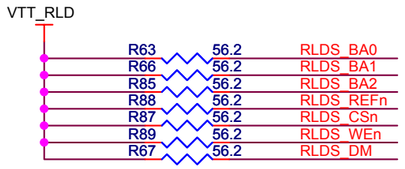
NOTE: THESE BYPASS CAPS ARE 0.1uF

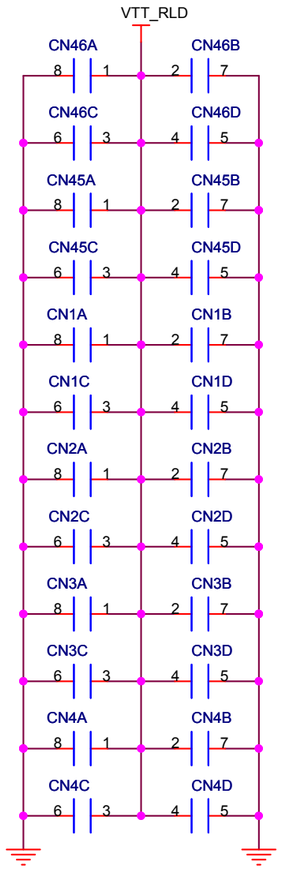
NOTE: THESE BYPASS CAPS ARE TO BE PLACED IN PARALLEL WITH EVERY OTHER VTT_RLD PULL UP RESISTOR.

PLACE THE RESISTORS WITHIN THIS BOX AS CLOSE AS POSSIBLE TO THE RLDRAM II SIO









NOTE: THESE BYPASS CAPS ARE 0.1uF

NOTE: THESE BYPASS CAPS ARE TO BE PLACED IN PARALLEL WITH EVERY OTHER VTT_RLD PULL UP RESISTOR.

RLDS_QK_P[1..0] RLDS_QK_P[1..0] 10,11
RLDS_BA[2..0] RLDS_BA[2..0] 10,11
RLDS_A[22..0] RLDS_A[22..0] 5,10,11
RLDS_D[17..0] RLDS_D[17..0] 10,11
RLDS_Q[17..0] RLDS_Q[17..0] 10,11

RLDS_QK_N[1..0] RLDS_QK_N[1..0] 10,11
RLDS_CSn RLDS_CSn 10,11
RLDS_WEn RLDS_WEn 10,11
RLDS_REFn RLDS_REFn 10,11
RLDS_DM RLDS_DM 10,11
RLDS_QVLD RLDS_QVLD 10,11

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RLDRAM II CIO 1

PLACE THESE RESISTORS AS CLOSE AS POSSIBLE TO THE RLDRAM II

VTT_RLD

RLDC_CK_P R306 56.2

RLDC_CK_N R305 56.2

U21B

5 RLDC_CK_P → RLDC_CK_P → J12 CK

5 RLDC_CK_N → RLDC_CK_N → K12 CK

K1 DK1

K2 DK1

VCCIO_RLD

R72 10K

RLDC_QK_P0 → D11 QK0

RLDC_QK_N0 → D10 QK0

RLDC_QK_P1 → R2 QK1

RLDC_QK_N1 → R3 QK1

RLDC_CSn → L2 CS

14,15 RLDC_WRITE_En → RLDC_WRITE_En → M1 WE

14,15 RLDC_REF_INn → RLDC_REF_INn → L1 REF

RLDC_DM → P12 DM

RLDC_QVLD → F12 QVLD

RLDC_BANK0 → J11 B0

RLDC_BANK1 → K11 B1

RLDC_BANK2 → H1 B2

A11 TMS

A12 TCK

V11 TDO

V12 TDI

R40 300

J23

J26 1 2 3

R47 250

V2 ZQ

VCCIO_RLD

Setting	Shunt Position
50 Ohms	J22,PIN1- J19,PIN2
60 Ohms	J19: PIN1-PIN2
MAX Drive	J19: PIN2-PIN3

RLDC_ADR0 → G12 A0

RLDC_ADR1 → G11 A1

RLDC_ADR2 → G10 A2

RLDC_ADR3 → H12 A3

RLDC_ADR4 → H11 A4

RLDC_ADR5 → F1 A5

RLDC_ADR6 → G2 A6

RLDC_ADR7 → G3 A7

RLDC_ADR8 → G1 A8

RLDC_ADR9 → H2 A9

RLDC_ADR10 → M12 A10

RLDC_ADR11 → M11 A11

RLDC_ADR12 → M10 A12

RLDC_ADR13 → L12 A13

RLDC_ADR14 → L11 A14

RLDC_ADR15 → P1 A15

RLDC_ADR16 → M2 A16

RLDC_ADR17 → M3 A17

RLDC_ADR18 → N1 A18

RLDC_ADR19 → N12 A19

RLDC_ADR20 → E12 A20

RLDC_ADR21 → E1 A21

RLDC_ADR22 → D1 A22

DNU0 B11

DNU1 C11

DNU2 E11

DNU3 F11

DNU4 B2

DNU5 C2

DNU6 D2

DNU7 E2

DNU8 F2

DNU9 N11

DNU10 P11

DNU11 R11

DNU12 T11

DNU13 U11

DNU14 N2

DNU15 P2

DNU16 T2

DNU17 U2

DQ0 B10 RLDC_DQ0

DQ1 C10 RLDC_DQ1

DQ2 E10 RLDC_DQ2

DQ3 F10 RLDC_DQ3

DQ4 B3 RLDC_DQ4

DQ5 C3 RLDC_DQ5

DQ6 D3 RLDC_DQ6

DQ7 E3 RLDC_DQ7

DQ8 F3 RLDC_DQ8

DQ9 N10 RLDC_DQ9

DQ10 P10 RLDC_DQ10

DQ11 R10 RLDC_DQ11

DQ12 T10 RLDC_DQ12

DQ13 U10 RLDC_DQ13

DQ14 N3 RLDC_DQ14

DQ15 P3 RLDC_DQ15

DQ16 T3 RLDC_DQ16

DQ17 U3 RLDC_DQ17

RLDRAM_II_CIO

U21A

1.8V

RLDC_VREF A1 VREF1

RLDC_VREF V1 VREF2

J1 NF1

J2 NF2

GND A2 VSS

A4 VSS

A9 VSS

D12 VSS

H3 VSS

H4 VSS

H9 VSS

H10 VSS

L3 VSS

L4 VSS

L9 VSS

L10 VSS

R1 VSS

R12 VSS

V4 VSS

V9 VSS

B4 VSSQ

B9 VSSQ

D4 VSSQ

D9 VSSQ

F4 VSSQ

F9 VSSQ

N4 VSSQ

N9 VSSQ

R4 VSSQ

R9 VSSQ

U4 VSSQ

U9 VSSQ

VDD B1

VDD B12

VDD G4

VDD G9

VDD J3

VDD J4

VDD J9

VDD J10

VDD K3

VDD K4

VDD K9

VDD K10

VDD M4

VDD M9

VDD U1

VDD U12

VCCIO_RLD

VDDQ C4

VDDQ C9

VDDQ E4

VDDQ E9

VDDQ P4

VDDQ P9

VDDQ T4

VDDQ T9

VTT_RLD

VTT C1

VTT C12

VTT T1

VTT T12

2.5V

VEXT A3

VEXT A10

VEXT V3

VEXT V10

RLDRAM_II_CIO

RLDC_QK_P[1..0] → RLDC_QK_P[1..0] 10,14

RLDC_QK_N[1..0] → RLDC_QK_N[1..0] 14

RLDC_CSn → RLDC_CSn 10,14

RLDC_DM → RLDC_DM 10,14

RLDC_QVLD → RLDC_QVLD 10,14

RLDC_BANK[2..0] → RLDC_BANK[2..0] 14,15

RLDC_ADR[22..0] → RLDC_ADR[22..0] 14,15

RLDC_DQ[17..0] → RLDC_DQ[17..0] 10,14

PLACE THESE RESISTORS AS CLOSE AS POSSIBLE TO THE RLDRAM

VCCIO_RLD

R81 4.7K RLDC_VREF R79 4.7K

C119 0.1uF

C90 0.1uF

HSTL1

BYPASS CAPS FOR RLDRAM II CIO

1.8V

C100 0.1uF C83 0.1uF C138 0.1uF C319 0.1uF

BYPASS CAPS FOR RLDRAM II CIO

VCCIO_RLD

C310 0.1uF C331 0.1uF

BYPASS CAPS FOR RLDRAM II CIO

2.5V

C137 0.1uF C82 0.1uF C139 0.1uF C84 0.1uF

BYPASS CAPS FOR RLDRAM II CIO

VTT_RLD

C114 0.1uF C91 0.1uF C346 0.1uF C301 0.1uF

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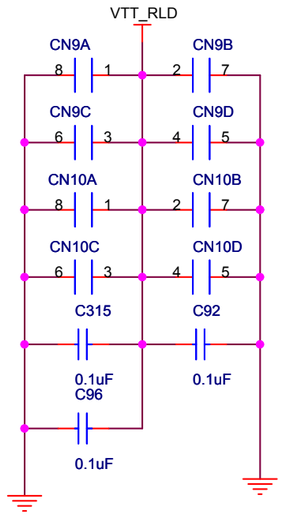
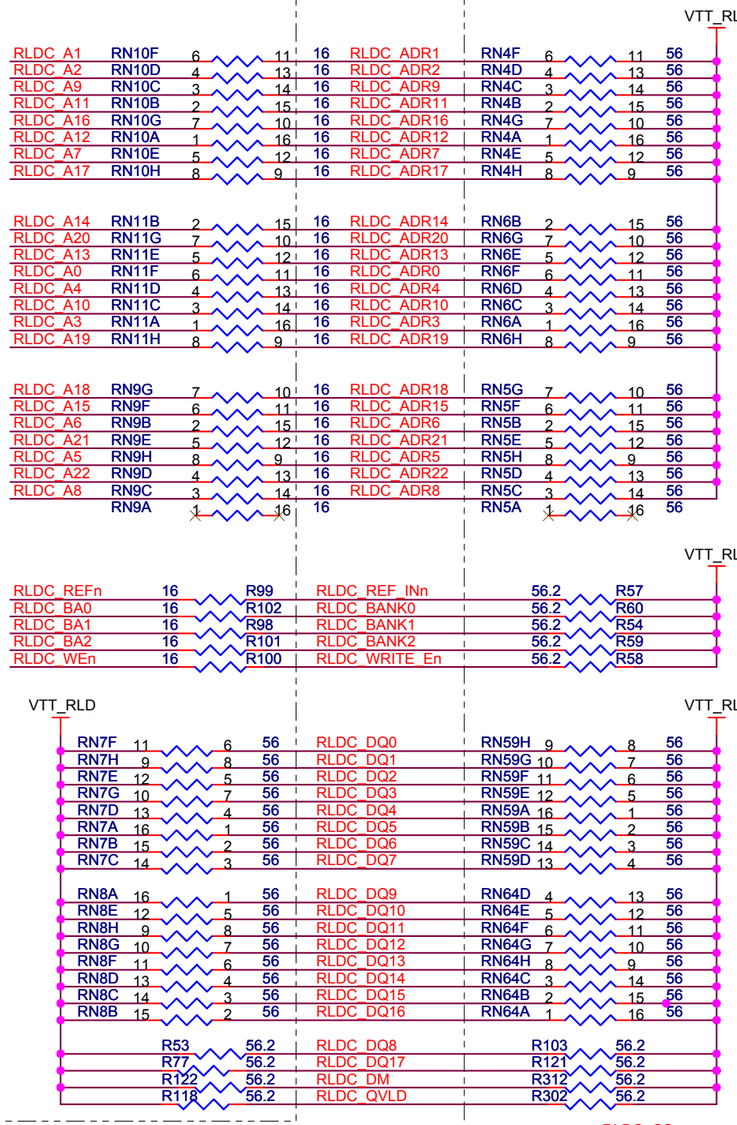
RLDRAM II CIO 1 Terminations

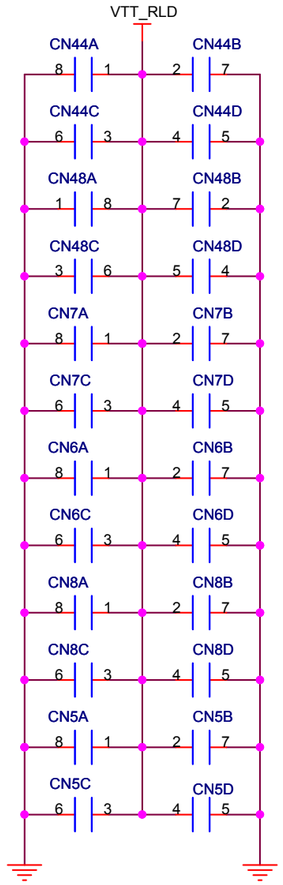
PLACE THE RESISTORS WITHIN THIS BOX AS CLOSE AS POSSIBLE TO THE STRATIX II DEVICE



NOTE: THE FOLLOWING BYPASS CAPS ARE 0.1uF
NOTE: THE FOLLOWING BYPASS CAPS ARE TO BE PLACED IN PARALLEL WITH EVERY OTHER 51 OR 51.1 OHM PULL UP RESISTOR.



PLACE THE RESISTORS WITHIN THIS BOX AS CLOSE AS POSSIBLE TO THE RLDRAM II CIO



NOTE: THE FOLLOWING BYPASS CAPS ARE 0.1uF
NOTE: THE FOLLOWING BYPASS CAPS ARE TO BE PLACED IN PARALLEL WITH EVERY OTHER 51 OR 51.1 OHM PULL UP RESISTOR

RLDC_WRITE_En → RLDC_WRITE_En 13,15
RLDC_REF_INn → RLDC_REF_INn 13,15
RLDC_CSn → RLDC_CSn 10,13
RLDC_WEn → RLDC_WEn 10
RLDC_REFn → RLDC_REFn 10
RLDC_DM → RLDC_DM 10,13
RLDC_QVLD → RLDC_QVLD 10,13

RLDC_ADR[22..0] → RLDC_ADR[22..0] 13,15
RLDC_BANK[2..0] → RLDC_BANK[2..0] 13,15
RLDC_BA[2..0] → RLDC_BA[2..0] 10
RLDC_A[22..0] → RLDC_A[22..0] 5,10
RLDC_DQ[17..0] → RLDC_DQ[17..0] 10,13
RLDC_QK_P[1..0] → RLDC_QK_P[1..0] 10,13
RLDC_QK_N[1..0] → RLDC_QK_N[1..0] 13

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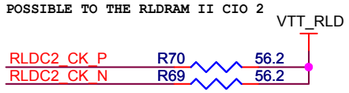
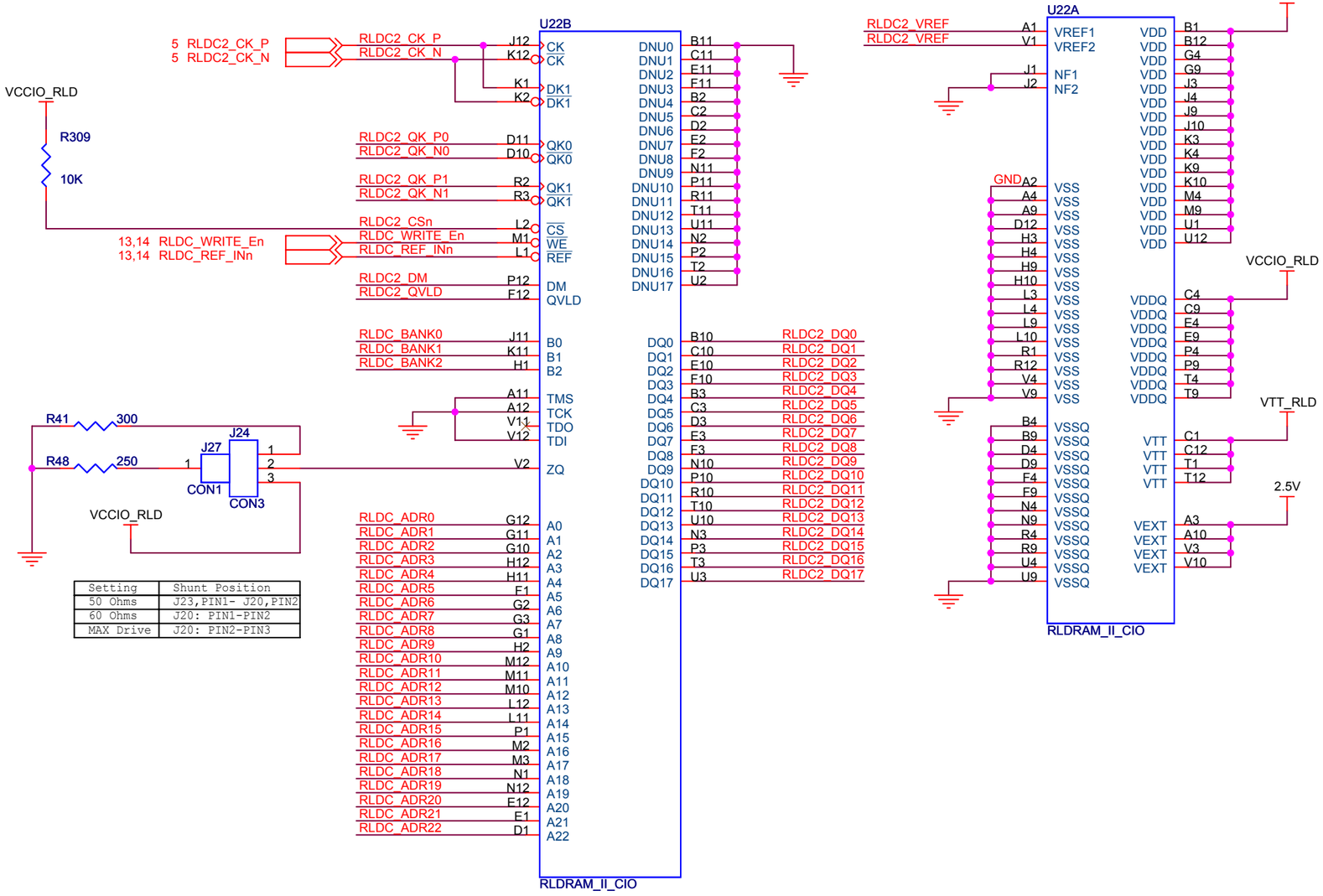
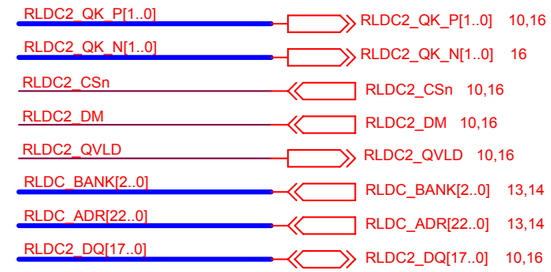
RLDRAM II CIO 2

PLACE THESE RESISTORS AS CLOSE AS POSSIBLE TO THE RLDRAM II CIO 2

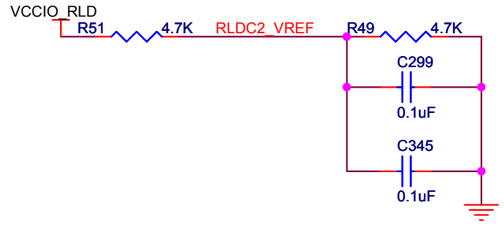




Setting	Shunt Position
50 Ohms	J23,PIN1- J20,PIN2
60 Ohms	J20: PIN1-PIN2
MAX Drive	J20: PIN2-PIN3

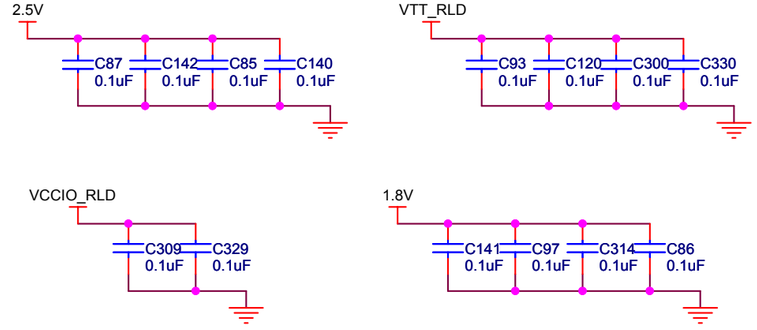


PLACE THESE RESISTORS AS CLOSE AS POSSIBLE TO THE RLDRAM



HSTL1

BYPASS CAPS FOR RLDRAM II CIO



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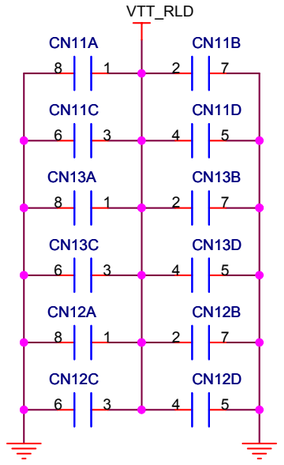
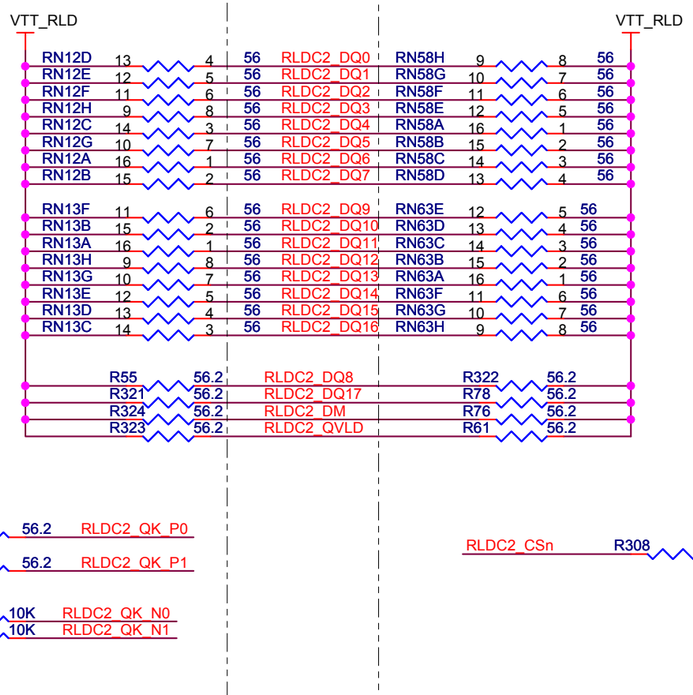
RLDRAM II CIO 2 Terminations

PLACE THE RESISTORS WITHIN THIS BOX AS
CLOSE AS POSSIBLE TO THE STRATIX II DEVICE

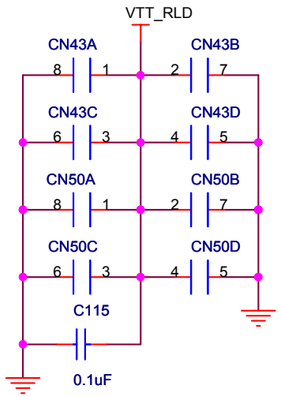


NOTE: THE FOLLOWING BYPASS CAPS
ARE 0.1uF

NOTE: THE FOLLOWING BYPASS CAPS ARE TO
BE PLACED IN PARALLEL WITH EVERY OTHER
51 OR 51.1 OHM PULL UP RESISTOR.



PLACE THE RESISTORS WITHIN THIS BOX AS
CLOSE AS POSSIBLE TO THE RLDRAM II CIO 2



NOTE: THE FOLLOWING BYPASS CAPS
ARE 0.1uF

NOTE: THE FOLLOWING BYPASS CAPS ARE TO
BE PLACED IN PARALLEL WITH EVERY OTHER
51 OR 51.1 OHM PULL UP RESISTOR.

RLDC2_DM → RLDC2_DM 10,15
RLDC2_CSn → RLDC2_CSn 10,15
RLDC2_QVLD → RLDC2_QVLD 10,15
RLDC2_DQ[17..0] → RLDC2_DQ[17..0] 10,15
RLDC2_QK_P[1..0] → RLDC2_QK_P[1..0] 10,15
RLDC2_QK_N[1..0] → RLDC2_QK_N[1..0] 15

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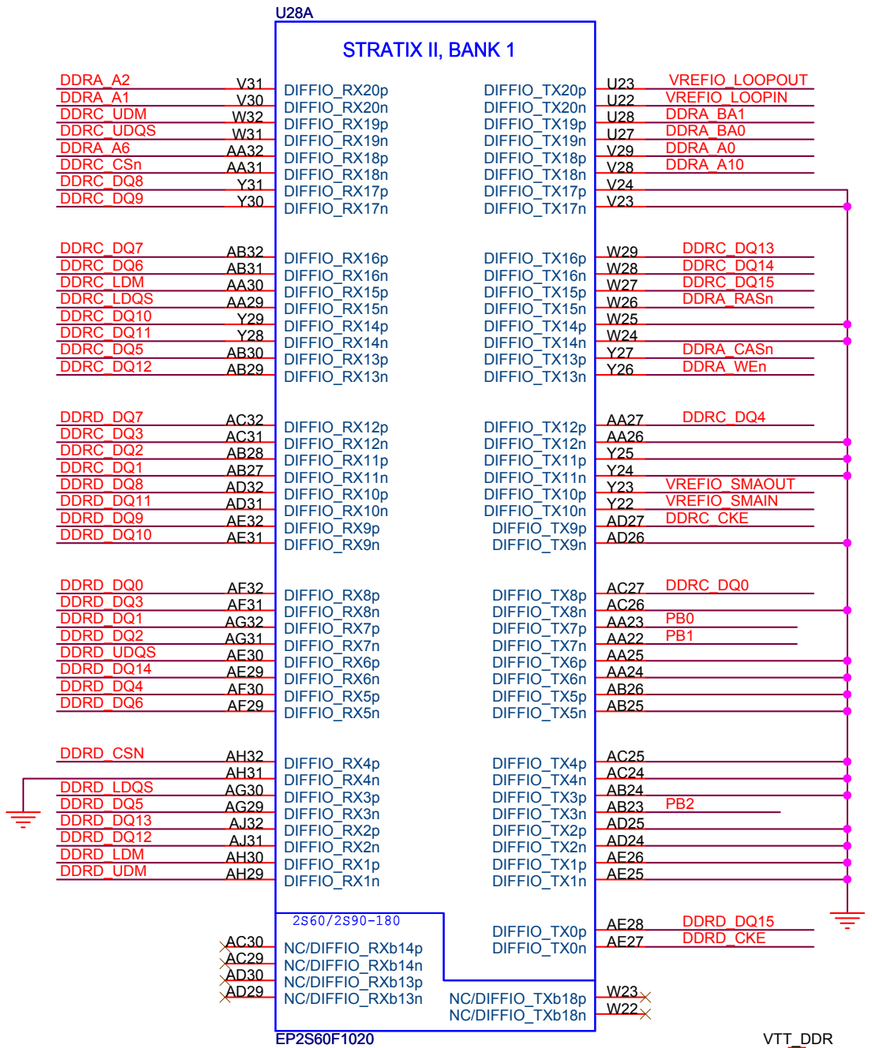
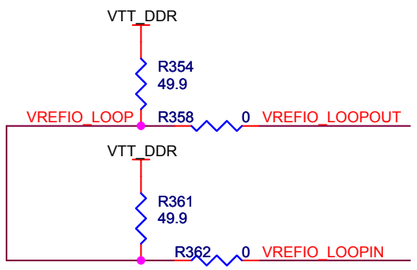
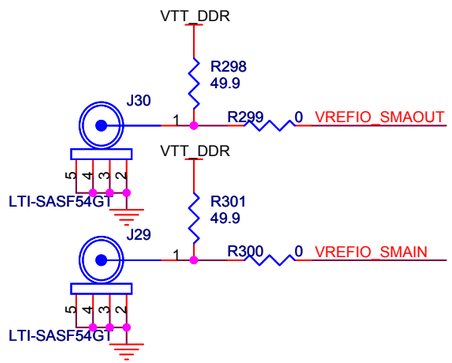
Stratix II Bank 1, Bank 2

Bank 1

(2.5V SSTL-2/2.5V LVCMOS)

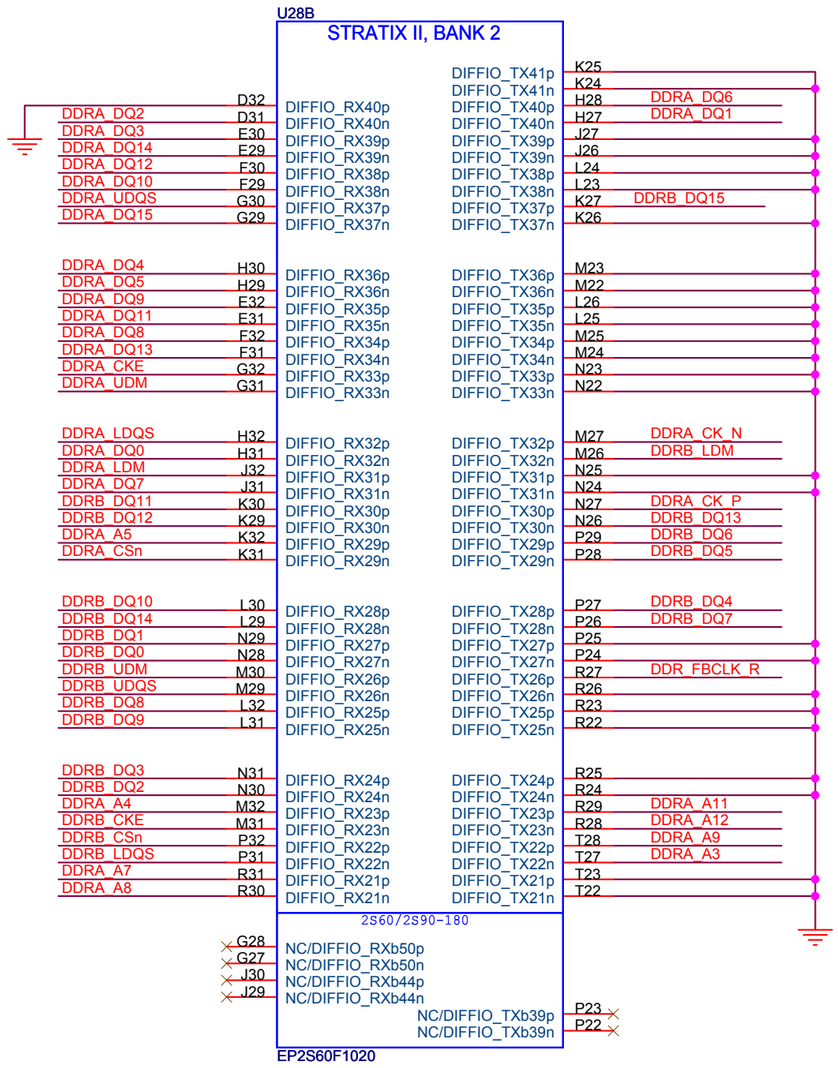






Bank 2

(2.5V SSTL-2/2.5V LVCMOS)



DDR DEVICES INTERFACES

DDR_FBCLK_R — DDR_FBCLK_R 20
DDRA_A[12..0] — DDRA_A[12..0] 19
DDRA_BA[1..0] — DDRA_BA[1..0] 19
DDRA_CK_P — DDRA_CK_P 18
DDRA_CK_N — DDRA_CK_N 18
DDRA_CASn — DDRA_CASn 19
DDRA_WEn — DDRA_WEn 19
DDRA_RASn — DDRA_RASn 19

DDRA INTERFACE

DDRA_DQ[15..0] — DDRA_DQ[15..0] 20
DDRA_CKE — DDRA_CKE 20
DDRA_CSn — DDRA_CSn 20
DDRA_LDM — DDRA_LDM 20
DDRA_UDM — DDRA_UDM 20
DDRA_LDQS — DDRA_LDQS 20
DDRA_UDQS — DDRA_UDQS 20

DDRB INTERFACE

DDRB_DQ[15..0] — DDRB_DQ[15..0] 20
DDRB_CKE — DDRB_CKE 20
DDRB_CSn — DDRB_CSn 20
DDRB_LDM — DDRB_LDM 20
DDRB_UDM — DDRB_UDM 20
DDRB_LDQS — DDRB_LDQS 20
DDRB_UDQS — DDRB_UDQS 20

DDRC INTERFACE

DDRC_DQ[15..0] — DDRC_DQ[15..0] 22
DDRC_CKE — DDRC_CKE 22
DDRC_CSn — DDRC_CSn 22
DDRC_LDM — DDRC_LDM 22
DDRC_UDM — DDRC_UDM 22
DDRC_LDQS — DDRC_LDQS 22
DDRC_UDQS — DDRC_UDQS 22

DDRD INTERFACE

DDRD_DQ[15..0] — DDRD_DQ[15..0] 22
DDRD_CKE — DDRD_CKE 22
DDRD_CSn — DDRD_CSn 22
DDRD_LDM — DDRD_LDM 22
DDRD_UDM — DDRD_UDM 22
DDRD_LDQS — DDRD_LDQS 22
DDRD_UDQS — DDRD_UDQS 22

PB[2..0] — PB[2..0] 33

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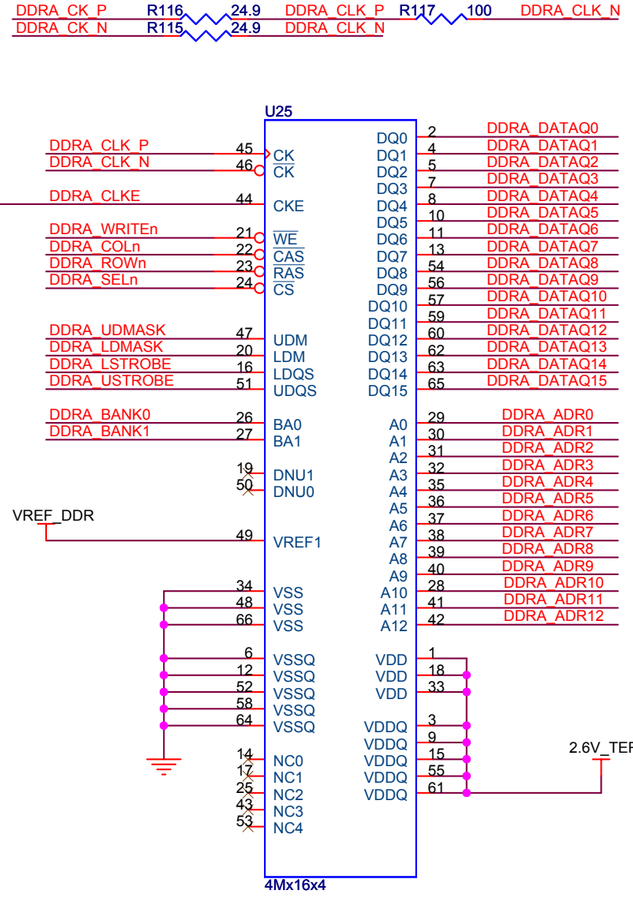
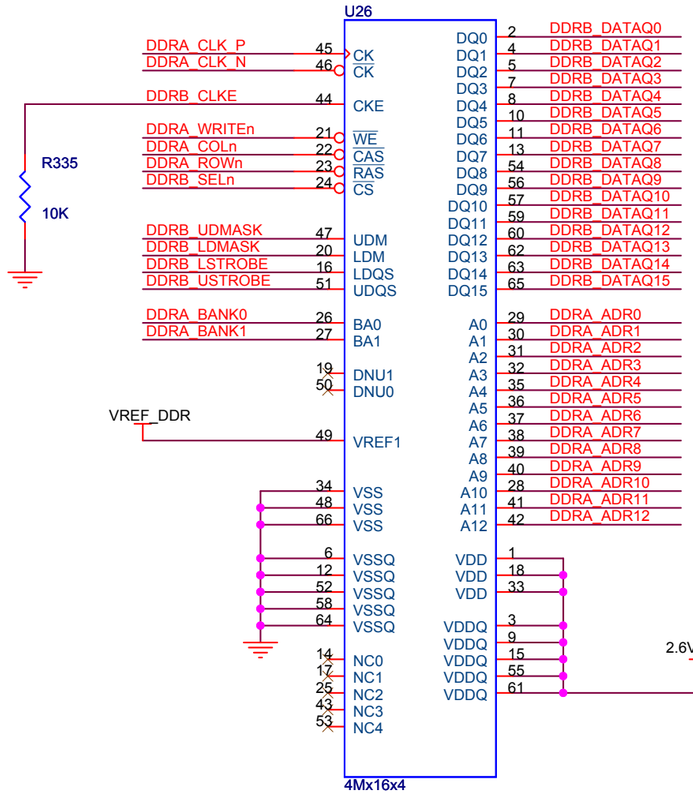
DDR SDRAM Page 1

Place this resistor as close
to the DDR SDRAM as possible





DDR SDRAM SHARED SIGNALS INTERFACE

DDRA_ADR[12..0] — DDRA_ADR[12..0] 19,21

DDRA_BANK[1..0] — DDRA_BANK[1..0] 19,21

DDRA_CLK_P — DDRA_CLK_P 21
DDRA_CLK_N — DDRA_CLK_N 21

DDRA_CK_P — DDRA_CK_P 17
DDRA_CK_N — DDRA_CK_N 17
DDRA_WRITEn — DDRA_WRITEn 19,21
DDRA_COLn — DDRA_COLn 19,21
DDRA_ROWn — DDRA_ROWn 19,21

DDRA INTERFACE

DDRA_DATAQ[15..0] — DDRA_DATAQ[15..0] 20

DDRA_CLKE — DDRA_CLKE 20
DDRA_SELn — DDRA_SELn 20
DDRA_UDMASK — DDRA_UDMASK 20
DDRA_LDMASK — DDRA_LDMASK 20

DDRA_USTROBE — DDRA_USTROBE 20
DDRA_LSTROBE — DDRA_LSTROBE 20

DDRB INTERFACE

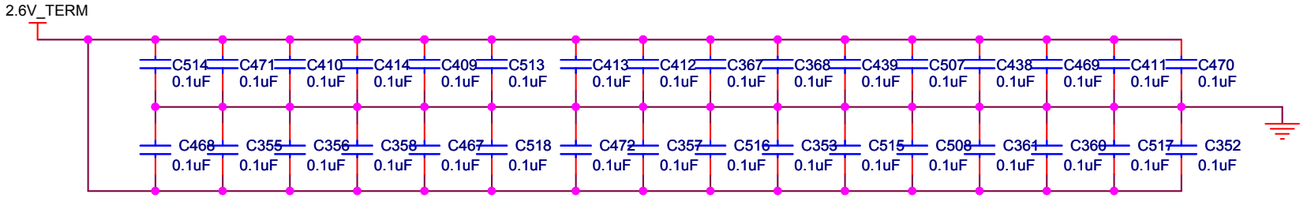
DDRB_DATAQ[15..0] — DDRB_DATAQ[15..0] 20

DDRB_CLKE — DDRB_CLKE 20
DDRB_SELn — DDRB_SELn 20
DDRB_UDMASK — DDRB_UDMASK 20
DDRB_LDMASK — DDRB_LDMASK 20

DDRB_USTROBE — DDRB_USTROBE 20
DDRB_LSTROBE — DDRB_LSTROBE 20

SSTL2

BYPASS CAPS FOR DDR SDRAM



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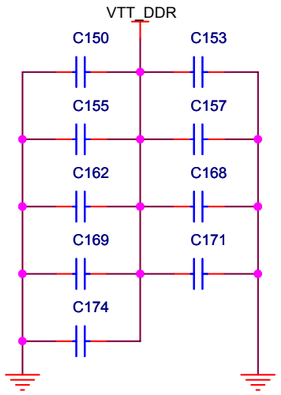
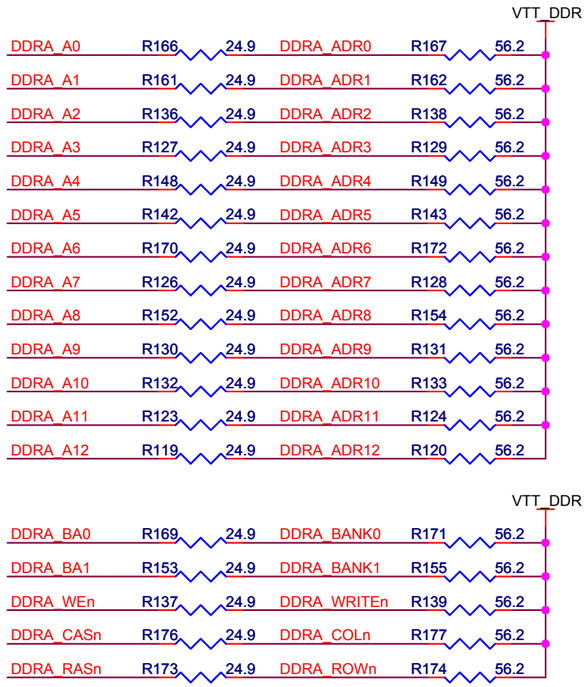
DDR SDRAM Terminations, Page 1 (Shared Signals Between All DDR SDRAMS)



NOTE: THE FOLLOWING BYPASS CAPS ARE 0.1uF

NOTE: THE FOLLOWING BYPASS CAPS ARE TO BE PLACED IN PARALLEL WITH EVERY OTHER 51.1 OHM PULL UP RESISTOR.



STRATIX II SIGNALS

DDRA_WEn — DDRA_WEn 17
DDRA_CASn — DDRA_CASn 17
DDRA_RASn — DDRA_RASn 17
DDRA_A[12..0] — DDRA_A[12..0] 17
DDRA_BA[1..0] — DDRA_BA[1..0] 17

DDR SDRAM SHARED SIGNALS

DDRA_WRITEn — DDRA_WRITEn 18,21
DDRA_COLn — DDRA_COLn 18,21
DDRA_ROWn — DDRA_ROWn 18,21
DDRA_ADR[12..0] — DDRA_ADR[12..0] 18,21
DDRA_BANK[1..0] — DDRA_BANK[1..0] 18,21

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DDR SDRAM A & B Terminations, Page 2

VTT_DDR

CN19A 8 1 — CN19B 2 7
CN19C 6 3 — CN19D 4 5
CN20A 8 1 — CN20B 2 7
CN20C 6 3 — CN20D 4 5
CN18A 8 1 — CN18B 2 7
CN18C 6 3 — CN18D 4 5
CN21A 8 1 — CN21B 2 7
CN21C 6 3 — CN21D 4 5
CN51A 8 1 — CN51B 2 7
CN51C 6 3 — CN51D 4 5
CN49A 1 8 — CN49B 7 2
CN49C 3 6 — CN49D 5 4
CN47A 8 1 — CN47B 2 7
CN47C 6 3 — CN47D 4 5
CN22A 8 1 — CN22B 2 7
CN22C 6 3 — CN22D 4 5
CN17A 1 8 — CN17B 7 2
CN17C 3 6 — CN17D 5 4
C474 — C453
C158 — C149

NOTE: THE FOLLOWING BYPASS CAPS ARE 0.1uF
NOTE: THE FOLLOWING BYPASS CAPS ARE TO BE PLACED IN PARALLEL WITH EVERY OTHER 51 OR 51.1 OHM PULL UP RESISTOR.

PLACE THE RESISTORS WITHIN THIS BOX AS CLOSE AS POSSIBLE TO THE STRATIX II DEVICE

VTT_DDR

DDRA_DQ0	RN20H	8	9	56
DDRA_DQ1	RN20G	7	10	56
DDRA_DQ2	RN20F	6	11	56
DDRA_DQ3	RN20E	5	12	56
DDRA_DQ4	RN20D	4	13	56
DDRA_DQ5	RN20C	3	14	56
DDRA_DQ6	RN20B	2	15	56
DDRA_DQ7	RN20A	1	16	56

VTT_DDR

DDRA_DQ8	RN18H	8	9	56
DDRA_DQ9	RN18E	5	12	56
DDRA_DQ10	RN18G	7	10	56
DDRA_DQ11	RN18D	4	13	56
DDRA_DQ12	RN18C	3	14	56
DDRA_DQ13	RN18F	6	11	56
DDRA_DQ14	RN18B	2	15	56
DDRA_DQ15	RN18A	1	16	56

VTT_DDR

DDRA_UDQS	R332	56.2
DDRA_LDQS	R342	56.2
DDRA_UDM	R327	56.2
DDRA_LDM	R348	56.2

VTT_DDR

DDRA_DQ0	RN19H	8	9	10
DDRA_DQ1	RN19G	7	10	10
DDRA_DQ2	RN19F	6	11	10
DDRA_DQ3	RN19E	5	12	10
DDRA_DQ4	RN19D	4	13	10
DDRA_DQ5	RN19C	3	14	10
DDRA_DQ6	RN19B	2	15	10
DDRA_DQ7	RN19A	1	16	10

VTT_DDR

DDRA_DQ8	RN17H	8	9	10
DDRA_DQ9	RN17E	5	12	10
DDRA_DQ10	RN17G	7	10	10
DDRA_DQ11	RN17D	4	13	10
DDRA_DQ12	RN17C	3	14	10
DDRA_DQ13	RN17F	6	11	10
DDRA_DQ14	RN17B	2	15	10
DDRA_DQ15	RN17A	1	16	10

VTT_DDR

DDRA_UDQS	R331	10
DDRA_LDQS	R340	10
DDRA_UDM	R326	10
DDRA_LDM	R343	10
DDRA_CKE	R339	10
DDRB_CKE	R360	10
DDRA_CSn	R349	10
DDRB_CSn	R363	10
DDR_FBCLK_R	R352	10

PLACE THE RESISTORS WITHIN THIS BOX AS CLOSE AS POSSIBLE TO THE DDR'S

VTT_DDR

DDRA_DATAQ0	RN66A	16	1	56
DDRA_DATAQ1	RN66B	15	2	56
DDRA_DATAQ2	RN66C	14	3	56
DDRA_DATAQ3	RN66D	13	4	56
DDRA_DATAQ4	RN66E	12	5	56
DDRA_DATAQ5	RN66F	11	6	56
DDRA_DATAQ6	RN66G	10	7	56
DDRA_DATAQ7	RN66H	9	8	56

VTT_DDR

DDRA_DATAQ8	RN62H	8	9	56
DDRA_DATAQ9	RN62G	7	10	56
DDRA_DATAQ10	RN62F	6	11	56
DDRA_DATAQ11	RN62E	5	12	56
DDRA_DATAQ12	RN62D	4	13	56
DDRA_DATAQ13	RN62C	3	14	56
DDRA_DATAQ14	RN62B	2	15	56
DDRA_DATAQ15	RN62A	1	16	56

VTT_DDR

DDRA_USTROBE	R316	56.2
DDRA_LSTROBE	R319	56.2
DDRA_UDMASK	R315	56.2
DDRA_LDMASK	R318	56.2
DDRA_CLKE	R314	56.2
DDRB_CLKE	R336	56.2
DDRA_SELn	R317	56.2
DDRB_SELn	R345	56.2
DDR_FBCLK	R357	56.2

PLACE THE RESISTORS WITHIN THIS BOX AS CLOSE AS POSSIBLE TO THE STRATIX II DEVICE

VTT_DDR

DDRB_DQ0	RN22E	5	12	56
DDRB_DQ1	RN22A	1	16	56
DDRB_DQ2	RN22B	2	15	56
DDRB_DQ3	RN22C	3	14	56
DDRB_DQ4	RN22H	8	9	56
DDRB_DQ5	RN22D	4	13	56
DDRB_DQ6	RN22F	6	11	56
DDRB_DQ7	RN22G	7	10	56

VTT_DDR

DDRB_DQ8	RN21B	2	15	56
DDRB_DQ9	RN21F	6	11	56
DDRB_DQ10	RN21C	3	14	56
DDRB_DQ11	RN21D	4	13	56
DDRB_DQ12	RN21A	1	16	56
DDRB_DQ13	RN21G	7	10	56
DDRB_DQ14	RN21E	5	12	56
DDRB_DQ15	RN21H	8	9	56

VTT_DDR

DDRB_UDQS	R355	56.2
DDRB_LDQS	R359	56.2
DDRB_UDM	R356	56.2
DDRB_LDM	R351	56.2

PLACE THE RESISTORS WITHIN THIS BOX AS CLOSE AS POSSIBLE TO THE DDR'S

VTT_DDR

DDRB_DQ0	RN68A	1	16	10
DDRB_DQ1	RN68B	2	15	10
DDRB_DQ2	RN68C	3	14	10
DDRB_DQ3	RN68D	4	13	10
DDRB_DQ4	RN68E	5	12	10
DDRB_DQ5	RN68F	6	11	10
DDRB_DQ6	RN68G	7	10	10
DDRB_DQ7	RN68H	8	9	10

VTT_DDR

DDRB_DQ8	RN67H	9	8	10
DDRB_DQ9	RN67G	10	7	10
DDRB_DQ10	RN67F	11	6	10
DDRB_DQ11	RN67E	12	5	10
DDRB_DQ12	RN67D	13	4	10
DDRB_DQ13	RN67C	14	3	10
DDRB_DQ14	RN67B	15	2	10
DDRB_DQ15	RN67A	16	1	10

VTT_DDR

DDRB_DATAQ0	RN23A	16	1	56
DDRB_DATAQ1	RN23B	15	2	56
DDRB_DATAQ2	RN23C	14	3	56
DDRB_DATAQ3	RN23D	13	4	56
DDRB_DATAQ4	RN23E	12	5	56
DDRB_DATAQ5	RN23F	11	6	56
DDRB_DATAQ6	RN23G	10	7	56
DDRB_DATAQ7	RN23H	9	8	56

VTT_DDR

DDRB_DATAQ8	RN16H	8	9	56
DDRB_DATAQ9	RN16G	7	10	56
DDRB_DATAQ10	RN16F	6	11	56
DDRB_DATAQ11	RN16E	5	12	56
DDRB_DATAQ12	RN16D	4	13	56
DDRB_DATAQ13	RN16C	3	14	56
DDRB_DATAQ14	RN16B	2	15	56
DDRB_DATAQ15	RN16A	1	16	56

VTT_DDR

DDRB_UDQS	R338	10
DDRB_LDQS	R347	10
DDRB_UDM	R337	10
DDRB_LDM	R346	10

DDRB_USTROBE	R113	56.2
DDRB_LSTROBE	R134	56.2
DDRB_UDMASK	R114	56.2
DDRB_LDMASK	R135	56.2

STRATIX II SIGNALS

DDR_FBCLK_R	DDR_FBCLK_R 17
DDR_FBCLK	DDR_FBCLK 5
DDRA_UDM	DDRA_UDM 17
DDRA_LDM	DDRA_LDM 17
DDRB_UDM	DDRB_UDM 17
DDRB_LDM	DDRB_LDM 17
DDRA_UDQS	DDRA_UDQS 17
DDRA_LDQS	DDRA_LDQS 17
DDRA_DQ[15..0]	DDRA_DQ[15..0] 17
DDRB_UDQS	DDRB_UDQS 17
DDRB_LDQS	DDRB_LDQS 17
DDRB_DQ[15..0]	DDRB_DQ[15..0] 17
DDRA_CKE	DDRA_CKE 17
DDRB_CKE	DDRB_CKE 17
DDRA_CSn	DDRA_CSn 17
DDRB_CSn	DDRB_CSn 17

DDR SDRAM A & B SIGNALS

DDRA_UDMASK	DDRA_UDMASK 18
DDRA_LDMASK	DDRA_LDMASK 18
DDRB_UDMASK	DDRB_UDMASK 18
DDRB_LDMASK	DDRB_LDMASK 18
DDRA_USTROBE	DDRA_USTROBE 18
DDRA_LSTROBE	DDRA_LSTROBE 18
DDRA_DATAQ[15..0]	DDRA_DATAQ[15..0] 18
DDRB_USTROBE	DDRB_USTROBE 18
DDRB_LSTROBE	DDRB_LSTROBE 18
DDRB_DATAQ[15..0]	DDRB_DATAQ[15..0] 18
DDRA_CLKE	DDRA_CLKE 18
DDRB_CLKE	DDRB_CLKE 18
DDRA_SELn	DDRA_SELn 18
DDRB_SELn	DDRB_SELn 18

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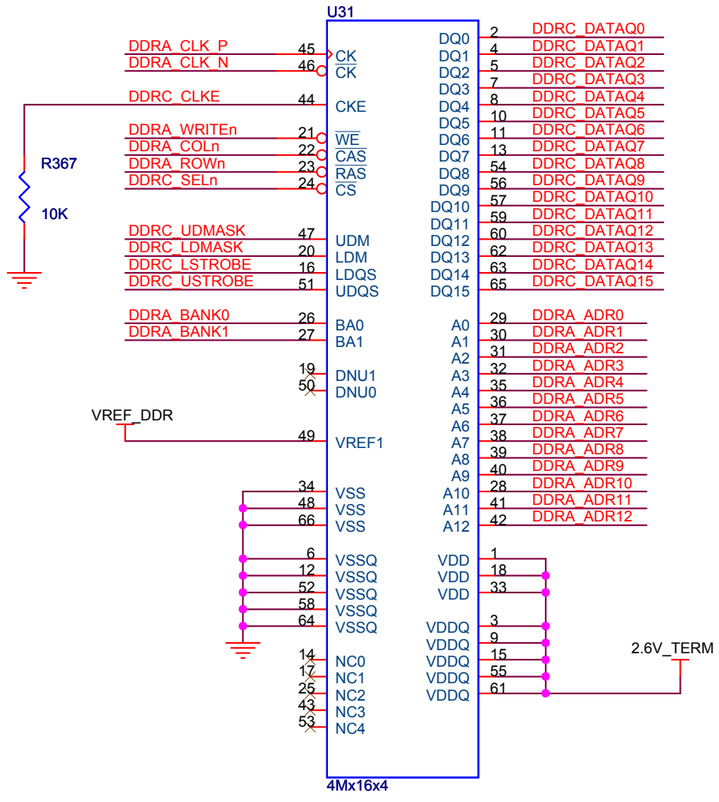
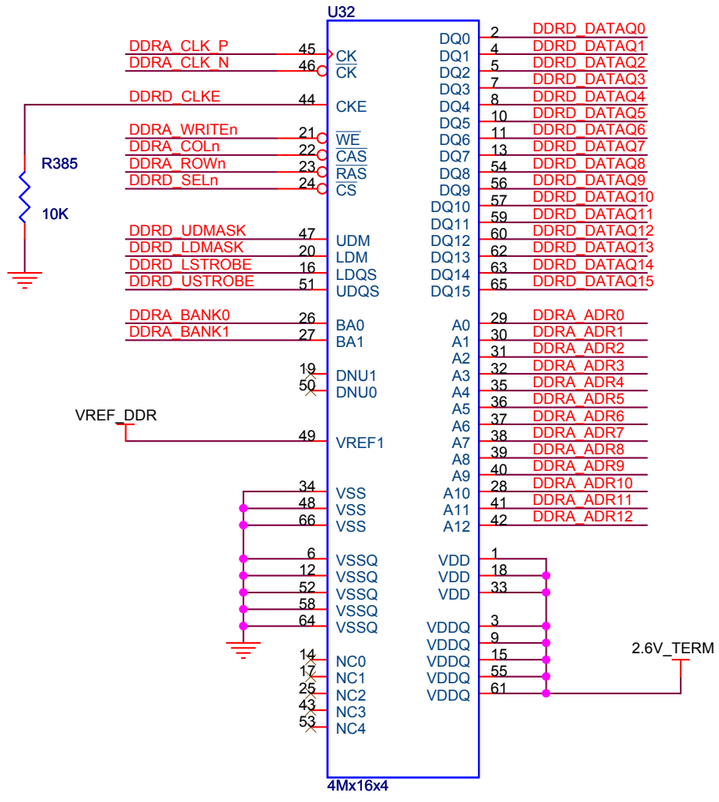
DDR SDRAM Page 2





DDR I SDRAM SHARED SIGNALS INTERFACE

DDRA_ADR[12..0] — DDRA_ADR[12..0] 18,19
DDRA_BANK[1..0] — DDRA_BANK[1..0] 18,19
DDRA_CLK_P — DDRA_CLK_P 18
DDRA_CLK_N — DDRA_CLK_N 18
DDRA_WRITEn — DDRA_WRITEn 18,19
DDRA_COLn — DDRA_COLn 18,19
DDRA_ROWn — DDRA_ROWn 18,19

DDRC INTERFACE

DDRC_DATAQ[15..0] — DDRC_DATAQ[15..0] 22
DDRC_CLKE — DDRC_CLKE 22
DDRC_SELn — DDRC_SELn 22
DDRC_UDMASK — DDRC_UDMASK 22
DDRC_LDMASK — DDRC_LDMASK 22
DDRC_USTROBE — DDRC_USTROBE 22
DDRC_LSTROBE — DDRC_LSTROBE 22

DDRD INTERFACE

DDRD_DATAQ[15..0] — DDRD_DATAQ[15..0] 22
DDRD_CLKE — DDRD_CLKE 22
DDRD_SELn — DDRD_SELn 22
DDRD_UDMASK — DDRD_UDMASK 22
DDRD_LDMASK — DDRD_LDMASK 22
DDRD_USTROBE — DDRD_USTROBE 22
DDRD_LSTROBE — DDRD_LSTROBE 22

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DDR SDRAM C & D Terminations, Page 3

VTT_DDR

CN53A 8 1 CN53B 2 7
CN53C 6 3 CN53D 4 5
CN52A 1 8 CN52B 7 2
CN52C 3 6 CN52D 5 4
CN26A 1 8 CN26B 7 2
CN26C 3 6 CN26D 5 4
CN33A 8 1 CN33B 2 7
CN33C 6 3 CN33D 4 5
CN23A 8 1 CN23B 2 7
CN23C 6 3 CN23D 4 5
CN24A 8 1 CN24B 2 7
CN24C 6 3 CN24D 4 5
CN25A 8 1 CN25B 2 7
CN25C 6 3 CN25D 4 5
CN27A 8 1 CN27B 2 7
CN27C 6 3 CN27D 4 5
C170 C167
C154 C151
C504 C450
C193 C503
C457 C194

PLACE THE RESISTORS WITHIN THIS BOX AS
CLOSE AS POSSIBLE TO THE STRATIX II DEVICE

DDRC_DQ0	RN28H	8	9	56	VTT_DDR
DDRC_DQ1	RN28D	4	13	56	
DDRC_DQ2	RN28F	6	11	56	
DDRC_DQ3	RN28E	5	12	56	
DDRC_DQ4	RN28G	7	10	56	
DDRC_DQ5	RN28C	3	14	56	
DDRC_DQ6	RN28B	2	15	56	
DDRC_DQ7	RN28A	1	16	56	

DDRC_DQ8	RN25E	5	12	56	VTT_DDR
DDRC_DQ9	RN25F	6	11	56	
DDRC_DQ10	RN25G	7	10	56	
DDRC_DQ11	RN25H	8	9	56	
DDRC_DQ12	RN25A	1	16	56	
DDRC_DQ13	RN25B	2	15	56	
DDRC_DQ14	RN25C	3	14	56	
DDRC_DQ15	RN25D	4	13	56	

				VTT_DDR
DDRC_UDQS	R365	56.2		
DDRC_LDQS	R371	56.2		
DDRC_UDM	R364	56.2		
DDRC_LDM	R366	56.2		

DDRC_DQ0	RN27H	8	9	10	VTT_DDR
DDRC_DQ1	RN27D	4	13	10	
DDRC_DQ2	RN27F	6	11	10	
DDRC_DQ3	RN27E	5	12	10	
DDRC_DQ4	RN27G	7	10	10	
DDRC_DQ5	RN27C	3	14	10	
DDRC_DQ6	RN27B	2	15	10	
DDRC_DQ7	RN27A	1	16	10	

DDRC_DQ8	RN24E	5	12	10	VTT_DDR
DDRC_DQ9	RN24F	6	11	10	
DDRC_DQ10	RN24G	7	10	10	
DDRC_DQ11	RN24H	8	9	10	
DDRC_DQ12	RN24A	1	16	10	
DDRC_DQ13	RN24B	2	15	10	
DDRC_DQ14	RN24C	3	14	10	
DDRC_DQ15	RN24D	4	13	10	

				VTT_DDR
DDRC_UDQS	R146	10		
DDRC_LDQS	R151	10		
DDRC_UDM	R141	10		
DDRC_LDM	R147	10		
DDRC_CKE	R373	10		
DDRD_CKE	R378	10		
DDRC_CSn	R372	10		
DDRD_CSn	R380	10		

PLACE THE RESISTORS WITHIN THIS BOX AS
CLOSE AS POSSIBLE TO THE DDR'S

DDRC_DATAQ0	RN70A	16	1	56	VTT_DDR
DDRC_DATAQ1	RN70B	15	2	56	
DDRC_DATAQ2	RN70C	14	3	56	
DDRC_DATAQ3	RN70D	13	4	56	
DDRC_DATAQ4	RN70E	12	5	56	
DDRC_DATAQ5	RN70F	11	6	56	
DDRC_DATAQ6	RN70G	10	7	56	
DDRC_DATAQ7	RN70H	9	8	56	

DDRC_DATAQ8	RN69H	8	9	56	VTT_DDR
DDRC_DATAQ9	RN69G	7	10	56	
DDRC_DATAQ10	RN69F	6	11	56	
DDRC_DATAQ11	RN69E	5	12	56	
DDRC_DATAQ12	RN69D	4	13	56	
DDRC_DATAQ13	RN69C	3	14	56	
DDRC_DATAQ14	RN69B	2	15	56	
DDRC_DATAQ15	RN69A	1	16	56	

				VTT_DDR
DDRC_USTROBE	R370	56.2		
DDRC_LSTROBE	R377	56.2		
DDRC_UDMASK	R369	56.2		
DDRC_LDMASK	R376	56.2		
DDRC_CLKE	R368	56.2		
DDRD_CLKE	R386	56.2		
DDRC_SELn	R375	56.2		
DDRD_SELn	R194	56.2		

PLACE THE RESISTORS WITHIN THIS BOX AS
CLOSE AS POSSIBLE TO THE STRATIX II DEVICE

DDRD_DQ0	RN36B	2	15	56	VTT_DDR
DDRD_DQ1	RN36F	6	11	56	
DDRD_DQ2	RN36H	8	9	56	
DDRD_DQ3	RN36A	1	16	56	
DDRD_DQ4	RN36D	4	13	56	
DDRD_DQ5	RN36G	7	10	56	
DDRD_DQ6	RN36C	3	14	56	
DDRD_DQ7	RN36E	5	12	56	

DDRD_DQ8	RN29A	1	16	56	VTT_DDR
DDRD_DQ9	RN29B	2	15	56	
DDRD_DQ10	RN29D	4	13	56	
DDRD_DQ11	RN29C	3	14	56	
DDRD_DQ12	RN29F	6	11	56	
DDRD_DQ13	RN29E	5	12	56	
DDRD_DQ14	RN29G	7	10	56	
DDRD_DQ15	RN29H	8	9	56	

				VTT_DDR
DDRD_UDQS	R374	56.2		
DDRD_LDQS	R379	56.2		
DDRD_UDM	R382	56.2		
DDRD_LDM	R381	56.2		

PLACE THE RESISTORS WITHIN THIS BOX AS
CLOSE AS POSSIBLE TO THE DDR'S

DDRD_DQ0	RN76A	1	16	10	VTT_DDR
DDRD_DQ1	RN76B	2	15	10	
DDRD_DQ2	RN76C	3	14	10	
DDRD_DQ3	RN76D	4	13	10	
DDRD_DQ4	RN76E	5	12	10	
DDRD_DQ5	RN76F	6	11	10	
DDRD_DQ6	RN76G	7	10	10	
DDRD_DQ7	RN76H	8	9	10	

DDRD_DQ8	RN71H	9	8	10	VTT_DDR
DDRD_DQ9	RN71G	10	7	10	
DDRD_DQ10	RN71F	11	6	10	
DDRD_DQ11	RN71E	12	5	10	
DDRD_DQ12	RN71D	13	4	10	
DDRD_DQ13	RN71C	14	3	10	
DDRD_DQ14	RN71B	15	2	10	
DDRD_DQ15	RN71A	16	1	10	

					VTT_DDR
DDRD_DATAQ0	RN37A	16	1	56	
DDRD_DATAQ1	RN37B	15	2	56	
DDRD_DATAQ2	RN37C	14	3	56	
DDRD_DATAQ3	RN37D	13	4	56	
DDRD_DATAQ4	RN37E	12	5	56	
DDRD_DATAQ5	RN37F	11	6	56	
DDRD_DATAQ6	RN37G	10	7	56	
DDRD_DATAQ7	RN37H	9	8	56	

					VTT_DDR
DDRD_DATAQ8	RN30H	8	9	56	
DDRD_DATAQ9	RN30G	7	10	56	
DDRD_DATAQ10	RN30F	6	11	56	
DDRD_DATAQ11	RN30E	5	12	56	
DDRD_DATAQ12	RN30D	4	13	56	
DDRD_DATAQ13	RN30C	3	14	56	
DDRD_DATAQ14	RN30B	2	15	56	
DDRD_DATAQ15	RN30A	1	16	56	

					VTT_DDR
DDRD_UDQS	R420	10	DDRD_USTROBE	R388	56.2
DDRD_LDQS	R434	10	DDRD_LSTROBE	R192	56.2
DDRD_UDM	R419	10	DDRD_UDMASK	R387	56.2
DDRD_LDM	R433	10	DDRD_LDMASK	R193	56.2

STRATIX II SIGNALS

DDRC_UDM	DDRC_UDM 17
DDRC_LDM	DDRC_LDM 17
DDRD_UDM	DDRD_UDM 17
DDRD_LDM	DDRD_LDM 17
DDRC_UDQS	DDRC_UDQS 17
DDRC_LDQS	DDRC_LDQS 17
DDRC_DQ[15..0]	DDRC_DQ[15..0] 17
DDRD_UDQS	DDRD_UDQS 17
DDRD_LDQS	DDRD_LDQS 17
DDRD_DQ[15..0]	DDRD_DQ[15..0] 17
DDRC_CKE	DDRC_CKE 17
DDRD_CKE	DDRD_CKE 17
DDRC_CSn	DDRC_CSn 17
DDRD_CSn	DDRD_CSn 17

DDR SDRAM C & D SIGNALS

DDRC_UDMASK	DDRC_UDMASK 21
DDRC_LDMASK	DDRC_LDMASK 21
DDRD_UDMASK	DDRD_UDMASK 21
DDRD_LDMASK	DDRD_LDMASK 21
DDRC_USTROBE	DDRC_USTROBE 21
DDRC_LSTROBE	DDRC_LSTROBE 21
DDRC_DATAQ[15..0]	DDRC_DATAQ[15..0] 21
DDRD_USTROBE	DDRD_USTROBE 21
DDRD_LSTROBE	DDRD_LSTROBE 21
DDRD_DATAQ[15..0]	DDRD_DATAQ[15..0] 21
DDRC_CLKE	DDRC_CLKE 21
DDRD_CLKE	DDRD_CLKE 21
DDRC_SELn	DDRC_SELn 21
DDRD_SELn	DDRD_SELn 21

NOTE: THE FOLLOWING BYPASS CAPS ARE 0.1uF

NOTE: THE FOLLOWING BYPASS CAPS ARE TO BE PLACED IN PARALLEL WITH EVERY OTHER 51 OR 51.1 OHM PULL UP RESISTOR.

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title	Stratix II Memory Board I	
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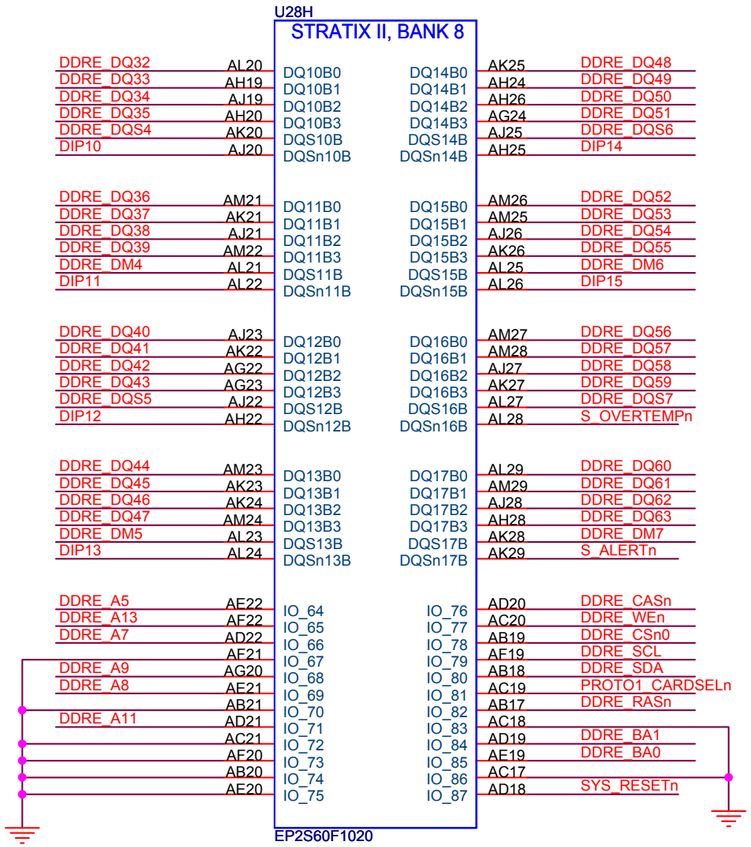
Stratix II Bank 7, Bank 8

Bank 7

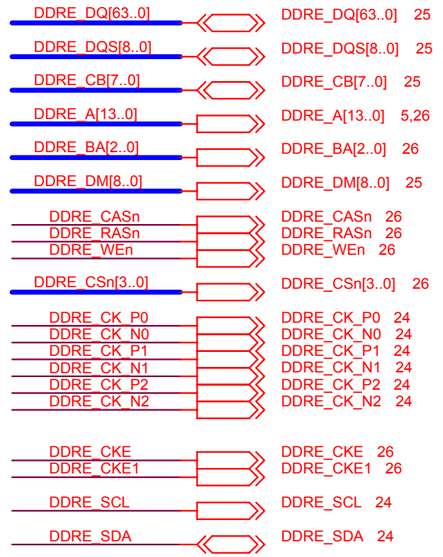
(2.5V SSTL-2 / 2.5V LVCMOS)

Bank 8

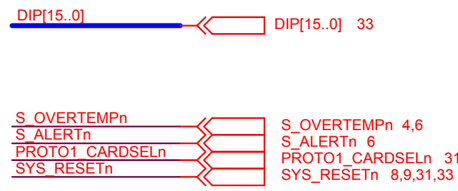
(2.5V SSTL-2 / 2.5V LVCMOS)



DDR DIMM INTERFACE



DIP SWITCHES



Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title	Stratix II Memory Board I	
Size: B	Document Number: 150-0310121-01	Rev: A
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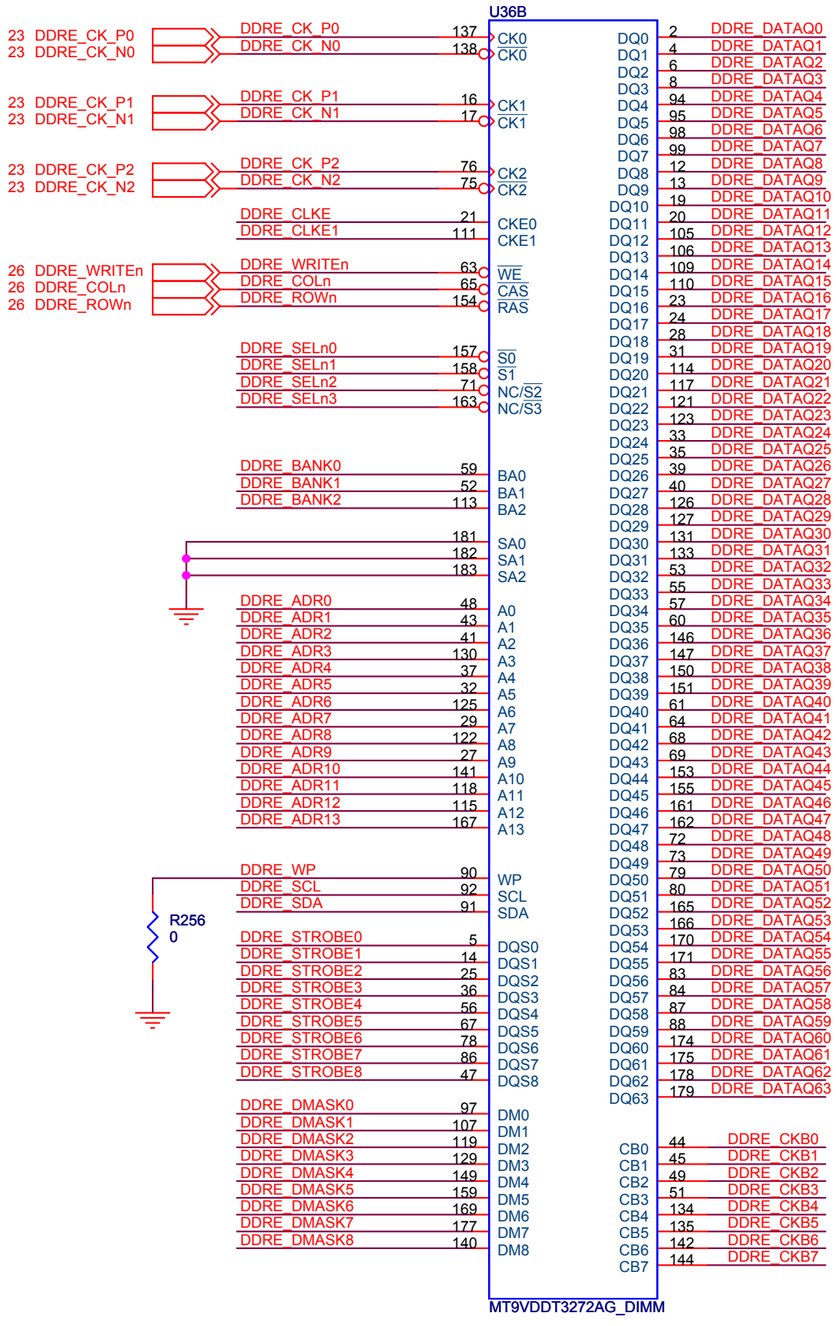
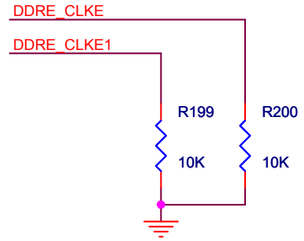
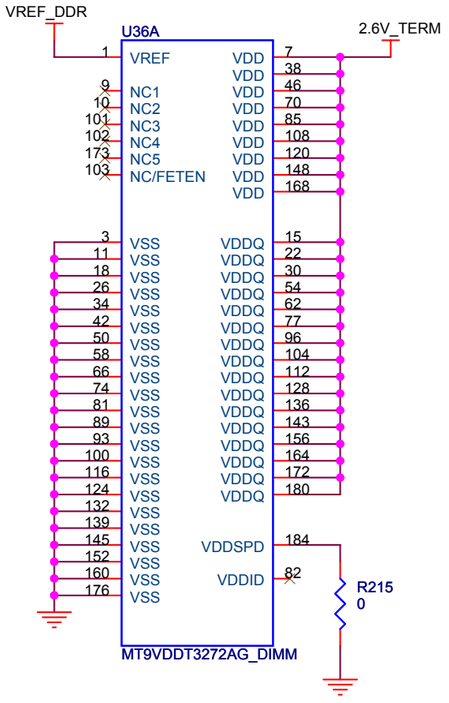
DDR SDRAM DIMM



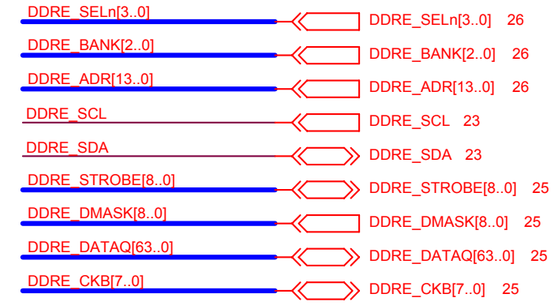




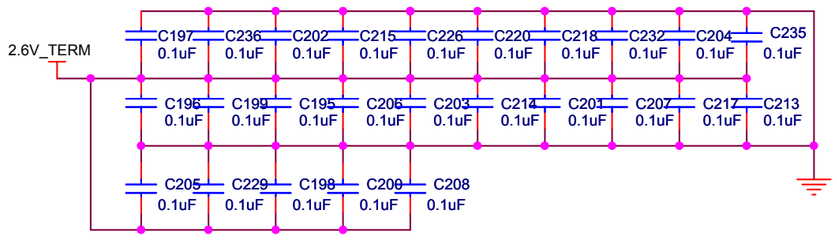
XU1

71243-3002

The DDR DIMM SOCKET IS FOR MICRON'S DIMM MODULE (MT8VDDT3264AG-40B)



BYPASS CAPS FOR DDR DIMM



Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title	Stratix II Memory Board I	
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DDR SDRAM DIMM Terminations Page 1

PLACE THESE COMPONENTS AS CLOSE AS POSSIBLE TO THE STRATIX II DEVICE

PLACE THESE COMPONENTS AS CLOSE AS POSSIBLE TO THE DDR DIMM

RN31H	9	8	56	DDRE_DQ0	RN38B	15	2	10	DDRE_DATAQ0	RN47C	14	3	56
RN31E	12	5	56	DDRE_DQ1	RN38D	13	4	10	DDRE_DATAQ1	RN47F	11	6	56
RN31F	11	6	56	DDRE_DQ2	RN38A	16	1	10	DDRE_DATAQ2	RN47G	10	7	56
RN31G	10	7	56	DDRE_DQ3	RN38C	14	3	10	DDRE_DATAQ3	RN47H	9	8	56
RN31B	15	2	56	DDRE_DQ4	RN38G	10	7	10	DDRE_DATAQ4	RN47A	16	1	56
RN31D	13	4	56	DDRE_DQ5	RN38E	12	5	10	DDRE_DATAQ5	RN47B	15	2	56
RN31C	14	3	56	DDRE_DQ6	RN38F	11	6	10	DDRE_DATAQ6	RN47D	13	4	56
RN31A	16	1	56	DDRE_DQ7	RN38H	9	8	10	DDRE_DATAQ7	RN47E	12	5	56
RN75C	14	3	56	DDRE_DQ8	RN39C	14	3	10	DDRE_DATAQ8	RN48A	16	1	56
RN75D	13	4	56	DDRE_DQ9	RN39D	13	4	10	DDRE_DATAQ9	RN48B	15	2	56
RN75A	16	1	56	DDRE_DQ10	RN39A	16	1	10	DDRE_DATAQ10	RN48G	10	7	56
RN75E	12	5	56	DDRE_DQ11	RN39E	12	5	10	DDRE_DATAQ11	RN48H	9	8	56
RN75G	10	7	56	DDRE_DQ12	RN39G	10	7	10	DDRE_DATAQ12	RN48C	14	3	56
RN75F	11	6	56	DDRE_DQ13	RN39F	11	6	10	DDRE_DATAQ13	RN48D	13	4	56
RN75B	15	2	56	DDRE_DQ14	RN39B	15	2	10	DDRE_DATAQ14	RN48E	12	5	56
RN75H	9	8	56	DDRE_DQ15	RN39H	9	8	10	DDRE_DATAQ15	RN48F	11	6	56
RN32D	13	4	56	DDRE_DQ16	RN40E	12	5	10	DDRE_DATAQ16	RN49B	15	2	56
RN32G	10	7	56	DDRE_DQ17	RN40B	15	2	10	DDRE_DATAQ17	RN49A	16	1	56
RN32H	9	8	56	DDRE_DQ18	RN40A	16	1	10	DDRE_DATAQ18	RN49E	12	5	56
RN32E	12	5	56	DDRE_DQ19	RN40D	13	4	10	DDRE_DATAQ19	RN49G	10	7	56
RN32A	16	1	56	DDRE_DQ20	RN40H	9	8	10	DDRE_DATAQ20	RN49C	14	3	56
RN32C	14	3	56	DDRE_DQ21	RN40F	11	6	10	DDRE_DATAQ21	RN49D	13	4	56
RN32F	11	6	56	DDRE_DQ22	RN40C	14	3	10	DDRE_DATAQ22	RN49F	11	6	56
RN32B	15	2	56	DDRE_DQ23	RN40G	10	7	10	DDRE_DATAQ23	RN49H	9	8	56
RN33D	13	4	56	DDRE_DQ24	RN41E	12	5	10	DDRE_DATAQ24	RN50A	16	1	56
RN33A	16	1	56	DDRE_DQ25	RN41H	9	8	10	DDRE_DATAQ25	RN50C	14	3	56
RN33H	9	8	56	DDRE_DQ26	RN41B	15	2	10	DDRE_DATAQ26	RN50G	10	7	56
RN33G	10	7	56	DDRE_DQ27	RN41A	16	1	10	DDRE_DATAQ27	RN50H	9	8	56
RN33C	14	3	56	DDRE_DQ28	RN41F	11	6	10	DDRE_DATAQ28	RN50B	15	2	56
RN33B	15	2	56	DDRE_DQ29	RN41G	10	7	10	DDRE_DATAQ29	RN50D	13	4	56
RN33F	11	6	56	DDRE_DQ30	RN41C	14	3	10	DDRE_DATAQ30	RN50E	12	5	56
RN33E	12	5	56	DDRE_DQ31	RN41D	13	4	10	DDRE_DATAQ31	RN50F	11	6	56
RN73D	13	4	56	DDRE_DQ32	RN43D	13	4	10	DDRE_DATAQ32	RN52A	16	1	56
RN73A	16	1	56	DDRE_DQ33	RN43B	15	2	10	DDRE_DATAQ33	RN52B	15	2	56
RN73B	15	2	56	DDRE_DQ34	RN43A	16	1	10	DDRE_DATAQ34	RN52E	12	5	56
RN73C	14	3	56	DDRE_DQ35	RN43C	14	3	10	DDRE_DATAQ35	RN52H	9	8	56
RN73E	12	5	56	DDRE_DQ36	RN43E	12	5	10	DDRE_DATAQ36	RN52C	14	3	56
RN73G	10	7	56	DDRE_DQ37	RN43G	10	7	10	DDRE_DATAQ37	RN52D	13	4	56
RN73H	9	8	56	DDRE_DQ38	RN43H	9	8	10	DDRE_DATAQ38	RN52F	11	6	56
RN73F	11	6	56	DDRE_DQ39	RN43F	11	6	10	DDRE_DATAQ39	RN52G	10	7	56
RN34E	12	5	56	DDRE_DQ40	RN44D	13	4	10	DDRE_DATAQ40	RN53B	15	2	56
RN34F	11	6	56	DDRE_DQ41	RN44C	14	3	10	DDRE_DATAQ41	RN53A	16	1	56
RN34H	9	8	56	DDRE_DQ42	RN44A	16	1	10	DDRE_DATAQ42	RN53E	12	5	56
RN34G	10	7	56	DDRE_DQ43	RN44B	15	2	10	DDRE_DATAQ43	RN53F	11	6	56
RN34D	13	4	56	DDRE_DQ44	RN44E	12	5	10	DDRE_DATAQ44	RN53C	14	3	56
RN34C	14	3	56	DDRE_DQ45	RN44F	11	6	10	DDRE_DATAQ45	RN53D	13	4	56
RN34A	16	1	56	DDRE_DQ46	RN44G	10	7	10	DDRE_DATAQ46	RN53G	10	7	56
RN34B	15	2	56	DDRE_DQ47	RN44H	9	8	10	DDRE_DATAQ47	RN53H	9	8	56
RN72D	13	4	56	DDRE_DQ48	RN45D	13	4	10	DDRE_DATAQ48	RN54A	16	1	56
RN72A	16	1	56	DDRE_DQ49	RN45A	16	1	10	DDRE_DATAQ49	RN54B	15	2	56
RN72H	9	8	56	DDRE_DQ50	RN45H	9	8	10	DDRE_DATAQ50	RN54G	10	7	56
RN72F	11	6	56	DDRE_DQ51	RN45F	11	6	10	DDRE_DATAQ51	RN54H	9	8	56
RN72C	14	3	56	DDRE_DQ52	RN45C	14	3	10	DDRE_DATAQ52	RN54D	13	4	56
RN72B	15	2	56	DDRE_DQ53	RN45B	15	2	10	DDRE_DATAQ53	RN54C	14	3	56
RN72G	10	7	56	DDRE_DQ54	RN45G	10	7	10	DDRE_DATAQ54	RN54E	12	5	56
RN72E	12	5	56	DDRE_DQ55	RN45E	12	5	10	DDRE_DATAQ55	RN54F	11	6	56
RN35F	11	6	56	DDRE_DQ56	RN46C	14	3	10	DDRE_DATAQ56	RN55C	14	3	56
RN35E	12	5	56	DDRE_DQ57	RN46D	13	4	10	DDRE_DATAQ57	RN55B	15	2	56
RN35H	9	8	56	DDRE_DQ58	RN46A	16	1	10	DDRE_DATAQ58	RN55G	10	7	56
RN35G	10	7	56	DDRE_DQ59	RN46B	15	2	10	DDRE_DATAQ59	RN55H	9	8	56
RN35D	13	4	56	DDRE_DQ60	RN46E	12	5	10	DDRE_DATAQ60	RN55A	16	1	56
RN35C	14	3	56	DDRE_DQ61	RN46F	11	6	10	DDRE_DATAQ61	RN55D	13	4	56
RN35B	15	2	56	DDRE_DQ62	RN46G	10	7	10	DDRE_DATAQ62	RN55E	12	5	56
RN35A	16	1	56	DDRE_DQ63	RN46H	9	8	10	DDRE_DATAQ63	RN55F	11	6	56

PLACE THESE COMPONENTS AS CLOSE AS POSSIBLE TO THE STRATIX II DEVICE

PLACE THESE COMPONENTS AS CLOSE AS POSSIBLE TO THE DDR DIMM

RN74C	14	3	56	DDRE_CB0	RN42C	14	3	10	DDRE_CKB0	RN51B	15	2	56
RN74B	15	2	56	DDRE_CB1	RN42B	15	2	10	DDRE_CKB1	RN51D	13	4	56
RN74A	16	1	56	DDRE_CB2	RN42A	16	1	10	DDRE_CKB2	RN51F	11	6	56
RN74H	9	8	56	DDRE_CB3	RN42H	9	8	10	DDRE_CKB3	RN51H	9	8	56
RN74E	12	5	56	DDRE_CB4	RN42E	12	5	10	DDRE_CKB4	RN51A	16	1	56
RN74G	10	7	56	DDRE_CB5	RN42G	10	7	10	DDRE_CKB5	RN51C	14	3	56
RN74F	11	6	56	DDRE_CB6	RN42F	11	6	10	DDRE_CKB6	RN51E	12	5	56
RN74D	13	4	56	DDRE_CB7	RN42D	13	4	10	DDRE_CKB7	RN51G	10	7	56

R418	56.2	DDRE_DM0	R195	10	DDRE_DMASK0	R218	56.2
R427	56.2	DDRE_DM1	R198	10	DDRE_DMASK1	R219	56.2
R180	56.2	DDRE_DM2	R202	10	DDRE_DMASK2	R226	56.2
R186	56.2	DDRE_DM3	R204	10	DDRE_DMASK3	R235	56.2
R423	56.2	DDRE_DM4	R208	10	DDRE_DMASK4	R243	56.2
R187	56.2	DDRE_DM5	R210	10	DDRE_DMASK5	R249	56.2
R432	56.2	DDRE_DM6	R212	10	DDRE_DMASK6	R252	56.2
R184	56.2	DDRE_DM7	R214	10	DDRE_DMASK7	R255	56.2
R426	56.2	DDRE_DM8	R205	10	DDRE_DMASK8	R240	56.2
R178	56.2	DDRE_DQS0	R196	10	DDRE_STROBE0	R217	56.2
R428	56.2	DDRE_DQS1	R197	10	DDRE_STROBE1	R220	56.2
R179	56.2	DDRE_DQS2	R201	10	DDRE_STROBE2	R224	56.2
R181	56.2	DDRE_DQS3	R203	10	DDRE_STROBE3	R231	56.2
R424	56.2	DDRE_DQS4	R207	10	DDRE_STROBE4	R242	56.2
R182	56.2	DDRE_DQS5	R209	10	DDRE_STROBE5	R250	56.2
R422	56.2	DDRE_DQS6	R211	10	DDRE_STROBE6	R253	56.2
R183	56.2	DDRE_DQS7	R213	10	DDRE_STROBE7	R254	56.2
R425	56.2	DDRE_DQS8	R206	10	DDRE_STROBE8	R239	56.2

DDRE_CB[7..0] — DDRE_CB[7..0] 23
DDRE_DQS[8..0] — DDRE_DQS[8..0] 23
DDRE_DM[8..0] — DDRE_DM[8..0] 23
DDRE_CKB[7..0] — DDRE_CKB[7..0] 24
DDRE_STROBE[8..0] — DDRE_STROBE[8..0] 24
DDRE_DMASK[8..0] — DDRE_DMASK[8..0] 24
DDRE_DATAQ[63..0] — DDRE_DATAQ[63..0] 24
DDRE_DQ[63..0] — DDRE_DQ[63..0] 23

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title	Stratix II Memory Board I	
Size: B	Document Number: 150-0310121-01	Rev: A
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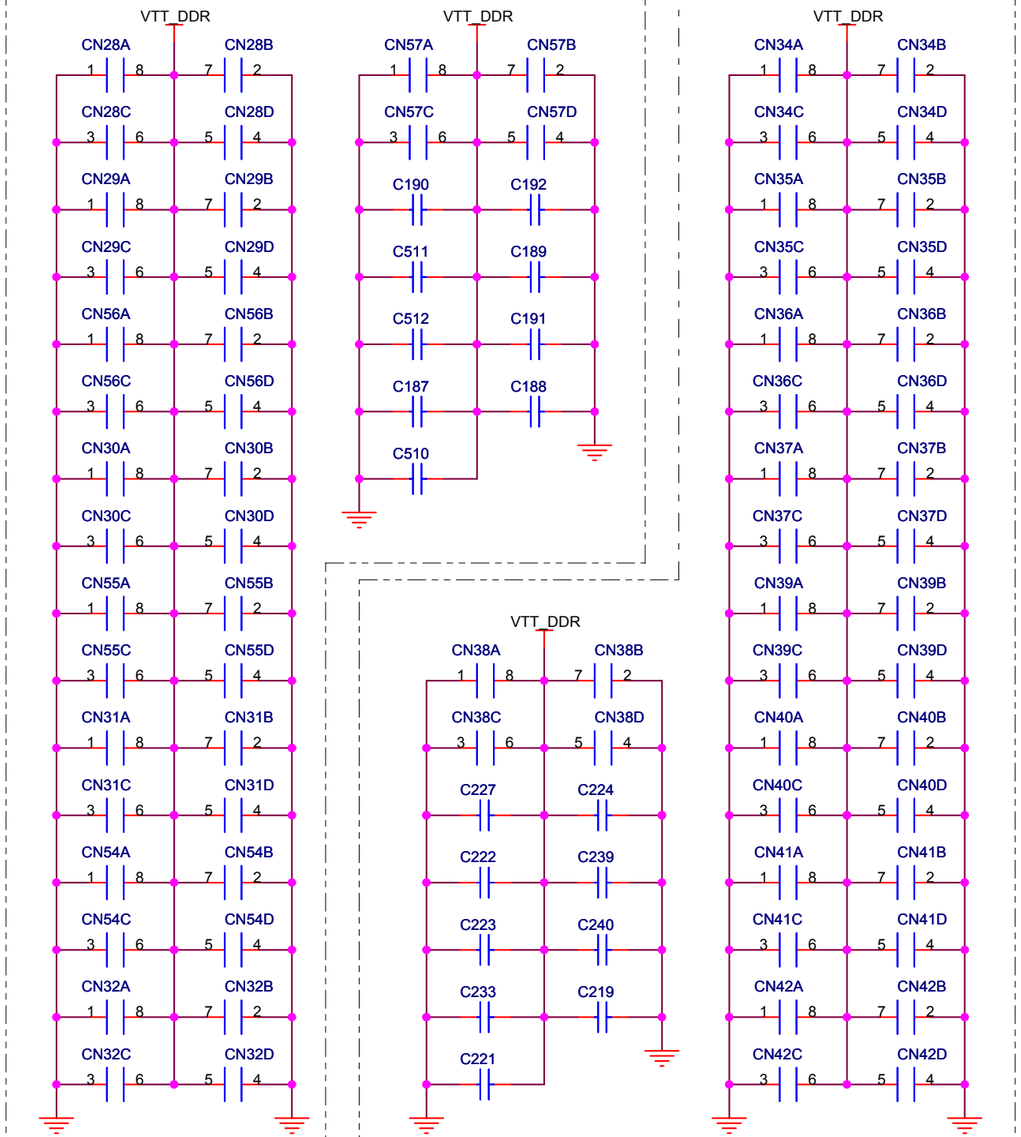
DDR SDRAM DIMM Terminations Page 2

NOTE: THE FOLLOWING BYPASS CAPS
ARE 0.1uF
NOTE: THE FOLLOWING BYPASS CAPS ARE TO
BE PLACED IN PARALLEL WITH EVERY OTHER
56 OR 56.2 OHM PULL UP RESISTOR.

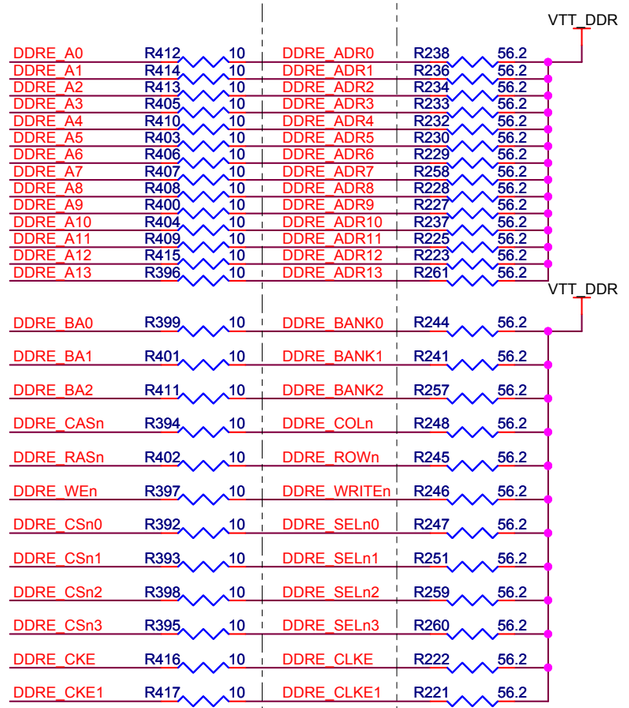
PLACE THESE COMPONENTS
AS CLOSE AS POSSIBLE TO
THE STRATIX II DEVICE

PLACE THE RESISTORS WITHIN
THIS BOX AS CLOSE AS
POSSIBLE TO THE DDR DIMM

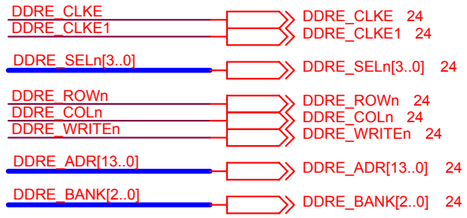


PLACE THE RESISTORS
WITHIN THIS BOX AS
CLOSE AS POSSIBLE TO
THE STRATIX II DEVICE

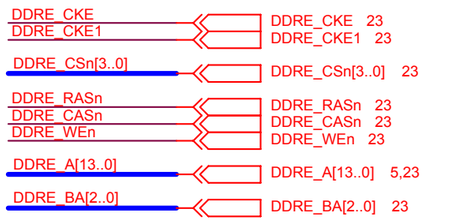
PLACE THE
RESISTORS WITHIN
THIS BOX AS CLOSE
AS POSSIBLE TO THE
DDR DIMM

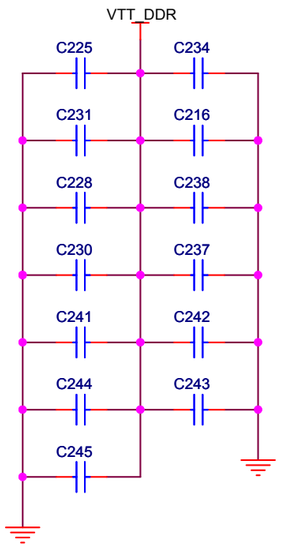


STRATIX INTERFACE



DDR SDRAM DIMM INTERFACE





NOTE: THE FOLLOWING BYPASS CAPS
ARE 0.1uF

NOTE: THE FOLLOWING BYPASS CAPS ARE TO
BE PLACED IN PARALLEL WITH EVERY OTHER
56.2 OHM PULL UP RESISTOR.

Altera Corporation, 9330 Scranton Rd #400, San Diego, CA 92121

Title		
Stratix II Memory Board I		
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Stratix II Bank 5, Bank 6

BANK 5
(3.3V LVTTL)

U28E
STRATIX II, BANK 5

FSE_A0	D1	DIFFIO_RX43p	DIFFIO_TX42p	J6	FSE_D0
FSE_A1	D2	DIFFIO_RX43n	DIFFIO_TX42n	J7	FSE_D1
FSE_A2	E3	DIFFIO_RX44p	DIFFIO_TX43p	J8	FSE_D2
FSE_A3	E4	DIFFIO_RX44n	DIFFIO_TX43n	J9	FSE_D3
FSE_A4	E1	DIFFIO_RX45p	DIFFIO_TX44p	K8	FSE_D4
FSE_A5	E2	DIFFIO_RX45n	DIFFIO_TX44n	K9	FSE_D5
FSE_A6	F3	DIFFIO_RX46p	DIFFIO_TX45p	L9	FSE_D6
FSE_A7	F4	DIFFIO_RX46n	DIFFIO_TX45n	L10	FSE_D7
			DIFFIO_TX46p	L7	FSE_D8
			DIFFIO_TX46n	L8	FSE_D9
FSE_A8	F1	DIFFIO_RX47p	DIFFIO_TX47p	K6	FSE_D10
FSE_A9	F2	DIFFIO_RX47n	DIFFIO_TX47n	K7	FSE_D11
FSE_A10	G3	DIFFIO_RX48p	DIFFIO_TX48p	L5	FSE_D12
FSE_A11	G4	DIFFIO_RX48n	DIFFIO_TX48n	L6	FSE_D13
FSE_A12	G1	DIFFIO_RX49p	DIFFIO_TX49p	M10	FSE_D14
FSE_A13	G2	DIFFIO_RX49n	DIFFIO_TX49n	M11	FSE_D15
FSE_A14	J3	DIFFIO_RX50p	DIFFIO_TX50p	M8	FSE_D16
FSE_A15	J4	DIFFIO_RX50n	DIFFIO_TX50n	M9	FSE_D17
FSE_A16	H1	DIFFIO_RX51p	DIFFIO_TX51p	M6	FSE_D18
FSE_A17	H2	DIFFIO_RX51n	DIFFIO_TX51n	M7	FSE_D19
FSE_A18	J1	DIFFIO_RX52p	DIFFIO_TX52p	N6	FSE_D20
FSE_A19	J2	DIFFIO_RX52n	DIFFIO_TX52n	N7	FSE_D21
FSE_A20	K3	DIFFIO_RX53p	DIFFIO_TX53p	N8	FSE_D22
FSE_A21	K4	DIFFIO_RX53n	DIFFIO_TX53n	N9	FSE_D23
FSE_A22	K1	DIFFIO_RX54p	DIFFIO_TX54p	P8	FSE_D24
FSE_A23	K2	DIFFIO_RX54n	DIFFIO_TX54n	P9	FSE_D25
FSE_A24	L3	DIFFIO_RX55p	DIFFIO_TX55p	P6	FSE_D26
FSE_A25	L4	DIFFIO_RX55n	DIFFIO_TX55n	P7	FSE_D27
FSE_A26	N4	DIFFIO_RX56p	DIFFIO_TX56p	P4	FSE_D28
FLASH_RESETn	N5	DIFFIO_RX56n	DIFFIO_TX56n	P5	FSE_D29
FLASH_RDY_BSYn	M3	DIFFIO_RX57p	DIFFIO_TX57p	P10	FSE_D30
FLASH_CEn	M4	DIFFIO_RX57n	DIFFIO_TX57n	P11	FSE_D31
FLASH_OEn	L1	DIFFIO_RX58p	DIFFIO_TX58p	R6	MAX_LED0
FLASH_WEn	L2	DIFFIO_RX58n	DIFFIO_TX58n	R7	MAX_LED1
SRAM_BEn0	N2	DIFFIO_RX59p	DIFFIO_TX59p	R4	MAX_LED2
SRAM_BEn1	N3	DIFFIO_RX59n	DIFFIO_TX59n	R5	MAX_LED3
SRAM_BEn2	M1	DIFFIO_RX60p	DIFFIO_TX60p	R10	MAX_LED4
SRAM_BEn3	M2	DIFFIO_RX60n	DIFFIO_TX60n	R11	MAX_LED5
SRAM_CSn	R2	DIFFIO_RX61p	DIFFIO_TX61p	T5	MAX_LED6
SRAM_OEn	R3	DIFFIO_RX61n	DIFFIO_TX61n	T6	MAX_LED7
SRAM_WEn	P1	DIFFIO_RX62p	DIFFIO_TX62p	T10	S_SMB_CLK
ENET_SRDYn	P2	DIFFIO_RX62n	DIFFIO_TX62n	T11	S_SMB_DATA

2S60/2S90-180

G5	NC/DIFFIO_RXb109p	NC/DIFFIO_TXb100p	N10
G6	NC/DIFFIO_RXb109n	NC/DIFFIO_TXb100n	N11
H3	NC/DIFFIO_RXb108p		
H4	NC/DIFFIO_RXb108n		

EP2S60F1020

BANK 6
(3.3V LVTTL)

U28F
STRATIX II, BANK 6

PROTO1_IO39	V2	DIFFIO_RX63p	DIFFIO_TX63p	U5	ENET_AEN
PROTO1_IO38	V3	DIFFIO_RX63n	DIFFIO_TX63n	U6	ENET_ADSn
PROTO1_IO37	W1	DIFFIO_RX64p	DIFFIO_TX64p	U10	ENET_BEn0
PROTO1_IO36	W2	DIFFIO_RX64n	DIFFIO_TX64n	U11	ENET_BEn1
PROTO1_IO35	Y2	DIFFIO_RX65p	DIFFIO_TX65p	V9	ENET_BEn2
PROTO1_IO34	Y3	DIFFIO_RX65n	DIFFIO_TX65n	V10	ENET_BEn3
PROTO1_IO33	AA1	DIFFIO_RX66p	DIFFIO_TX66p	V6	ENET_CYCLEn
PROTO1_IO32	AA2	DIFFIO_RX66n	DIFFIO_TX66n	V7	ENET_DATACSn
PROTO1_IO31	AA3	DIFFIO_RX67p	DIFFIO_TX67p	V4	ENET_INTRQ0
PROTO1_IO30	AA4	DIFFIO_RX67n	DIFFIO_TX67n	V5	ENET_IOCHRDY
PROTO1_IO29	Y4	DIFFIO_RX68p	DIFFIO_TX68p	W8	ENET_IORn
PROTO1_IO28	Y5	DIFFIO_RX68n	DIFFIO_TX68n	W9	ENET_IOWn
PROTO1_IO27	AB1	DIFFIO_RX69p	DIFFIO_TX69p	W6	ENET_VLBUSn
PROTO1_IO26	AB2	DIFFIO_RX69n	DIFFIO_TX69n	W7	ENET_LCLK
PROTO1_IO25	AB3	DIFFIO_RX70p	DIFFIO_TX70p	W4	ENET_LDEVn
PROTO1_IO24	AB4	DIFFIO_RX70n	DIFFIO_TX70n	W5	ENET_RDYRTNn
PROTO1_IO23	AC1	DIFFIO_RX71p	DIFFIO_TX71p	Y6	ENET_W_Rn
PROTO1_IO22	AC2	DIFFIO_RX71n	DIFFIO_TX71n	Y7	RS232A_TXD
PROTO1_IO21	AC3	DIFFIO_RX72p	DIFFIO_TX72p	Y8	RS232A_RTS
PROTO1_IO20	AC4	DIFFIO_RX72n	DIFFIO_TX72n	Y9	RS232A_RXD
PROTO1_IO19	AD1	DIFFIO_RX73p	DIFFIO_TX73p	Y10	RS232A_CTS
PROTO1_IO18	AD2	DIFFIO_RX73n	DIFFIO_TX73n	Y11	RS232B_TXD
PROTO1_IO17	AE1	DIFFIO_RX74p	DIFFIO_TX74p	AB5	RS232B_RTS
PROTO1_IO16	AE2	DIFFIO_RX74n	DIFFIO_TX74n	AB6	RS232B_RXD
PROTO1_IO15	AE3	DIFFIO_RX75p	DIFFIO_TX75p	AA10	RS232B_CTS
PROTO1_IO14	AE4	DIFFIO_RX75n	DIFFIO_TX75n	AA11	DIG_1_DP
PROTO1_IO13	AF1	DIFFIO_RX76p	DIFFIO_TX76p	AA6	DIG_1_G
PROTO1_IO12	AF2	DIFFIO_RX76n	DIFFIO_TX76n	AA7	DIG_1_F
PROTO1_IO11	AF3	DIFFIO_RX77p	DIFFIO_TX77p	AD6	DIG_1_E
PROTO1_IO10	AF4	DIFFIO_RX77n	DIFFIO_TX77n	AD7	DIG_1_D
PROTO1_IO9	AG1	DIFFIO_RX78p	DIFFIO_TX78p	AA8	DIG_1_C
PROTO1_IO8	AG2	DIFFIO_RX78n	DIFFIO_TX78n	AA9	DIG_1_B
PROTO1_IO7	AG3	DIFFIO_RX79p	DIFFIO_TX79p	AC6	DIG_1_A
PROTO1_IO6	AG4	DIFFIO_RX79n	DIFFIO_TX79n	AC7	DIG_2_DP
PROTO1_IO5	AH1	DIFFIO_RX80p	DIFFIO_TX80p	AB7	DIG_2_G
PROTO1_IO4	AH2	DIFFIO_RX80n	DIFFIO_TX80n	AB8	DIG_2_F
PROTO1_IO3	AH3	DIFFIO_RX81p	DIFFIO_TX81p	AB9	DIG_2_E
PROTO1_IO2	AH4	DIFFIO_RX81n	DIFFIO_TX81n	AB10	DIG_2_D
PROTO1_IO1	AJ1	DIFFIO_RX82p	DIFFIO_TX82p	AC8	DIG_2_C
PROTO1_IO0	AJ2	DIFFIO_RX82n	DIFFIO_TX82n	AC9	DIG_2_B
			DIFFIO_TX83p	AD8	DIG_2_A
			DIFFIO_TX83n	AD9	PROTO1_IO40

2S60/2S90-180

AD3	NC/DIFFIO_RXb73p	NC/DIFFIO_TXb77p	W10
AD4	NC/DIFFIO_RXb73n	NC/DIFFIO_TXb77n	W11
AE5	NC/DIFFIO_RXb69p		
AE6	NC/DIFFIO_RXb69n		

EP2S60F1020

SEVEN SEGMENT DISPLAY

DIG_1_DP	DIG_1_DP 32
DIG_1_G	DIG_1_G 32
DIG_1_F	DIG_1_F 32
DIG_1_E	DIG_1_E 32
DIG_1_D	DIG_1_D 32
DIG_1_C	DIG_1_C 32
DIG_1_B	DIG_1_B 32
DIG_1_A	DIG_1_A 32
DIG_2_DP	DIG_2_DP 32
DIG_2_G	DIG_2_G 32
DIG_2_F	DIG_2_F 32
DIG_2_E	DIG_2_E 32
DIG_2_D	DIG_2_D 32
DIG_2_C	DIG_2_C 32
DIG_2_B	DIG_2_B 32
DIG_2_A	DIG_2_A 32

SRAM INTERFACE

SRAM_BEn[3..0]	SRAM_BEn[3..0] 28
SRAM_CSn	SRAM_CSn 28
SRAM_OEn	SRAM_OEn 28
SRAM_WEn	SRAM_WEn 28

SHARED BUS AND FLASH INTERFACE

FSE_D[31..0]	FSE_D[31..0] 8,9,28,29
FSE_A[26..0]	FSE_A[26..0] 8,9,28,29
FLASH_CEn	FLASH_CEn 8,9,28
FLASH_OEn	FLASH_OEn 8,9,28
FLASH_WEn	FLASH_WEn 8,9,28
FLASH_RDY_BSYn	FLASH_RDY_BSYn 8,9,28
FLASH_RESETn	FLASH_RESETn 8,9,28

DEBUG PORT

PROTO1_IO[40..0]	PROTO1_IO[40..0] 31

RS-232 INTERFACE

RS232A_TXD	RS232A_TXD 30
RS232A_CTS	RS232A_CTS 30
RS232A_RXD	RS232A_RXD 30
RS232A_RTS	RS232A_RTS 30
RS232B_TXD	RS232B_TXD 30
RS232B_CTS	RS232B_CTS 30
RS232B_RXD	RS232B_RXD 30
RS232B_RTS	RS232B_RTS 30

LED, DIPSWITCH INTERFACE

MAX_LED[7..0]	MAX_LED[7..0] 8,9
PB[2..0]	PB[2..0] 17,33

ETHERNET/MAC INTERFACE

ENET_BEn[3..0]	ENET_BEn[3..0] 29
ENET_ADSn	ENET_ADSn 29
ENET_AEN	ENET_AEN 29
ENET_IORn	ENET_IORn 29
ENET_IOWn	ENET_IOWn 29
ENET_IOCHRDY	ENET_IOCHRDY 29
ENET_LDEVn	ENET_LDEVn 29
ENET_CYCLEn	ENET_CYCLEn 29
ENET_INTRQ0	ENET_INTRQ0 29
ENET_RDYRTNn	ENET_RDYRTNn 29
ENET_DATACSn	ENET_DATACSn 29
ENET_W_Rn	ENET_W_Rn 29
ENET_LCLK	ENET_LCLK 29
ENET_SRDYn	ENET_SRDYn 29
ENET_VLBUSn	ENET_VLBUSn 29
S_SMB_CLK	S_SMB_CLK 6
S_SMB_DATA	S_SMB_DATA 6

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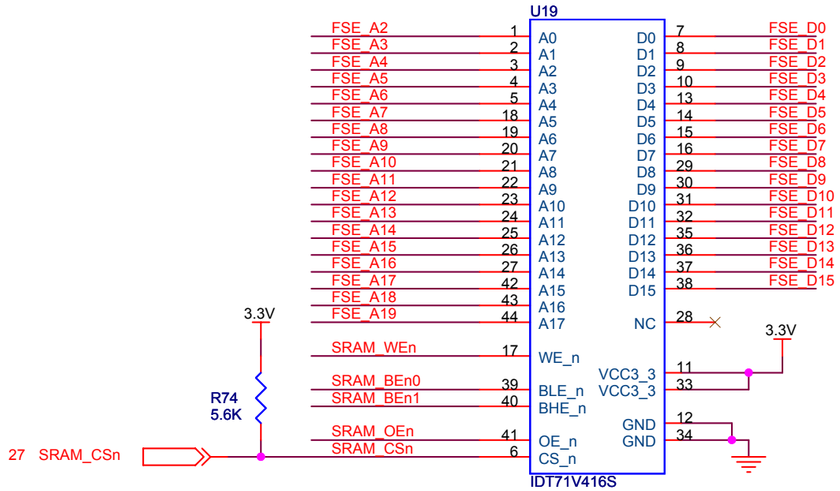
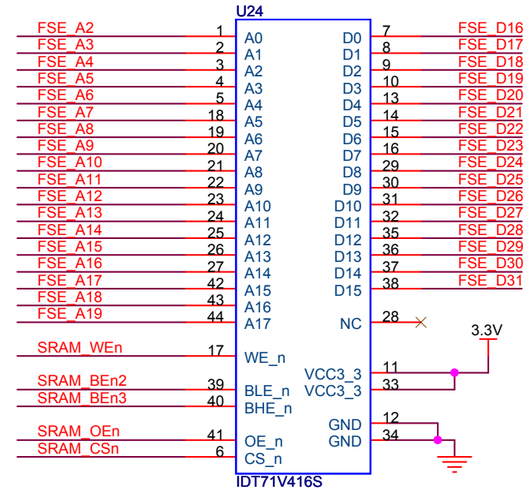
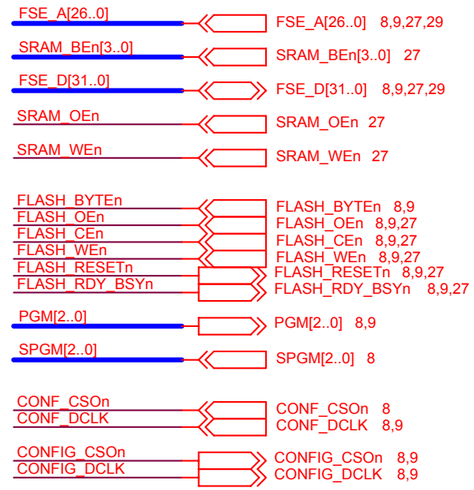
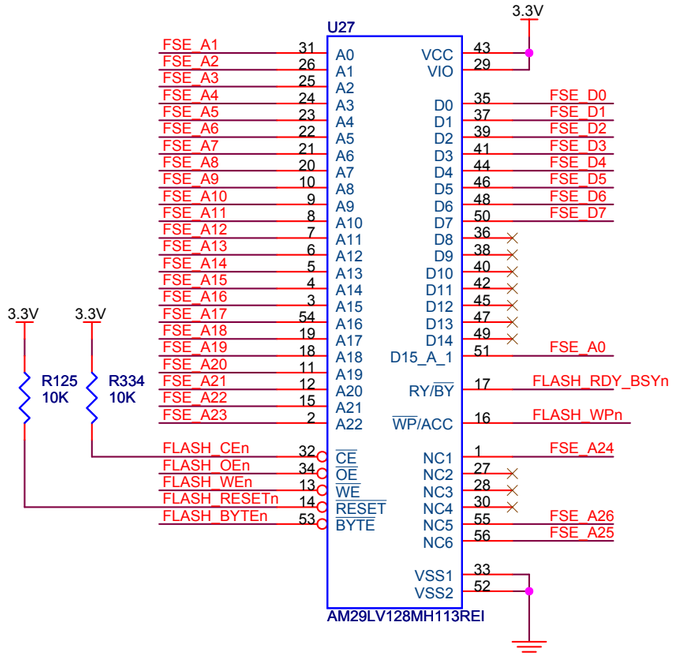
SRAM, Flash Memory and Voltage Translators

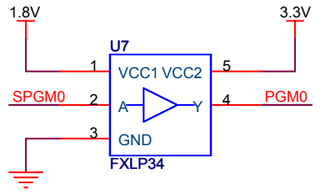


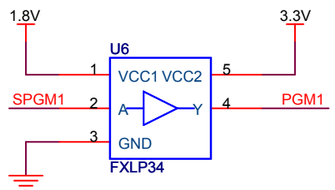


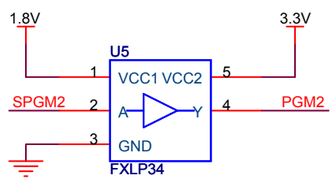
One bank of 256K x 32 SRAM (two 256K x 16 parts in parallel) = 1Mbyte of SRAM

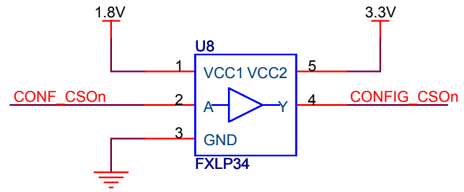


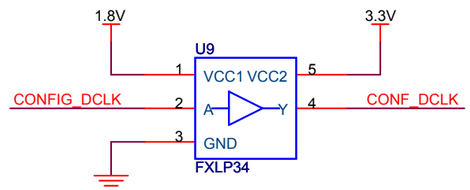


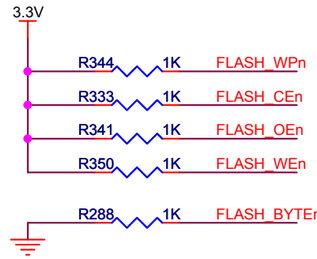


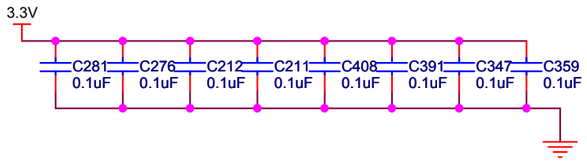












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10/100 Ethernet Interface

MAC/PHY

LAN91C111

U20

3.3V_LAN

VDD x8 (1, 33, 44, 62, 77, 98, 110, 120)

AVDD x2 (11, 16)

MII INTERFACE PINS

ENET_BEn3	97	BE3#
ENET_BEn2	96	BE2#
ENET_BEn1	95	BE1#
ENET_BEn0	94	BE0#
ENET_AEN	41	AEN
FSE_A1	78	A1
FSE_A2	79	A2
FSE_A3	80	A3
FSE_A4	81	A4
FSE_A5	82	A5
FSE_A6	83	A6
FSE_A7	84	A7
FSE_A8	85	A8
FSE_A9	86	A9
FSE_A10	87	A10
FSE_A11	88	A11
FSE_A12	89	A12
FSE_A13	90	A13
FSE_A14	91	A14
FSE_A15	92	A15
FSE_D0	107	D0
FSE_D1	106	D1
FSE_D2	105	D2
FSE_D3	104	D3
FSE_D4	102	D4
FSE_D5	101	D5
FSE_D6	100	D6
FSE_D7	99	D7
FSE_D8	76	D8
FSE_D9	75	D9
FSE_D10	74	D10
FSE_D11	73	D11
FSE_D12	71	D12
FSE_D13	70	D13
FSE_D14	69	D14
FSE_D15	68	D15
FSE_D16	66	D16
FSE_D17	65	D17
FSE_D18	64	D18
FSE_D19	63	D19
FSE_D20	61	D20
FSE_D21	60	D21
FSE_D22	59	D22
FSE_D23	58	D23
FSE_D24	56	D24
FSE_D25	55	D25
FSE_D26	54	D26
FSE_D27	53	D27
FSE_D28	51	D28
FSE_D29	50	D29
FSE_D30	49	D30
FSE_D31	48	D31

INTERFACE PINS

ENET_RESET	30	RESET
ENET_ADSn	37	ADS#
ENET_LCLK	42	LCLK
ENET_IOCHRDY	38	ARDY
ENET_RDYRTNn	46	RDYRTN#
ENET_SRDYn	43	SRDY#
ENET_INTRQ0	29	INTR0
ENET_LDEVn	45	LDEV#
ENET_IORn	31	RD#
ENET_IOWn	32	WR#
ENET_DATACSn	34	DATACS#
ENET_CYCLEn	35	CYCLE#
ENET_W_Rn	36	W/R#
ENET_VLBUSn	40	VLBUS#

VSS x10 (24, 39, 52, 57, 67, 72, 93, 103, 108, 117)

AVSS x2 (13, 19)

PHY

TPO+	14	
TPO-	15	
TPI+	17	
TPI-	18	
LNK#	20	
LBK	21	
CNTRL#	28	
RBIAS	12	
LEDA#	22	
LEDB#	23	

MII INTERFACE

RXD3	121	
RXD2	122	
RXD1	123	
RXD0	124	
TXD3	113	
TXD2	114	
TXD1	115	
TXD0	116	
TXEN100	111	
CRS100	119	
COL100	112	
RXDV	125	
RXER	126	
MDI	25	
MDO	26	
MCLK	27	
RX25	118	
TX25	109	

SERIAL EEPROM

IOS0	3	
IOS1	4	
IOS2	5	
ENEEP	6	
ENDO	7	
ENDI	8	
EESK	9	
EECS	10	

XTAL2	128	
XTAL1	127	
CSOUT#	2	
X25OUT	47	

3.3V_LAN

C320 0.01uF X7R

R307 24.9

R311 24.9

R56 49.9

R68 49.9

ENET_TXDN

ENET_TXDP

R71 24.9 ENET_RXDP

R73 24.9 ENET_RXDN

R310 0

ENET_RBIAS

R304 11K

ENET_LEDA_n

ENET_LEDB_n

ENET_ENEEP

R303 250

CLK_25MHZ

Integrated RJ45
(includes LEDs and magnetics)

RJ1

OCT	8		
NC0	7		
TDN	3	D4	12
TDP	1		
TCT	2	D3	11
RCT	5		
RDN	6	D2	10
RDP	4		
		D1	9

SMNT1 14, MNT0 15, SMNT0 13, MNT1 16

C118 0.001uF X7R

VCCA

3.3V_LAN

ENET_LEDB_n

ENET_LEDA_n

3.3V

L10 47nH

C111 0.1uF

C107 0.001uF X7R

C79 1uF X7R

3.3V

L8 1.5A/330

C75 10uF 10V Tantalum

C302 0.1uF, C326 0.1uF, C303 0.1uF, C348 0.1uF, C316 0.1uF, C311 0.1uF, C304 0.1uF, C350 0.1uF

C321 0.01uF, C76 0.01uF, C349 0.1uF

3.3V_LAN

ENET_CYCLEn	RN65A	1 / 16 10K
ENET_W_Rn	RN65B	2 / 15 10K
ENET_RDYRTNn	RN65C	3 / 14 10K
ENET_IOWn	RN65D	4 / 13 10K
ENET_OSC_EN	RN65E	5 / 12 10K
ENET_ADSn	RN65F	6 / 11 10K
ENET_LCLK	RN65G	7 / 10 10K
ENET_IORn	RN65H	8 / 9 10K

3.3V_LAN

X1

1	EN	OUT	4
2	NC1	NC2	5
3	GND	VCC	6

CRYSTAL
Fox Electronics
JITO 2_DS3AE_25.000

CLK_25MHZ

ENET_BEn[3..0] — ENET_BEn[3..0] 27

FSE_D[31..0] — FSE_D[31..0] 8,9,27,28

FSE_A[26..0] — FSE_A[26..0] 8,9,27,28

ENET_RESET — ENET_RESET 8,9

ENET_DATACSn — ENET_DATACSn 27

ENET_AEN — ENET_AEN 27

ENET_IORn — ENET_IORn 27

ENET_IOWn — ENET_IOWn 27

ENET_IOCHRDY — ENET_IOCHRDY 27

ENET_LDEVn — ENET_LDEVn 27

ENET_SRDYn — ENET_SRDYn 27

ENET_INTRQ0 — ENET_INTRQ0 27

ENET_VLBUSn — ENET_VLBUSn 27

ENET_ADSn — ENET_ADSn 27

ENET_LCLK — ENET_LCLK 27

ENET_W_Rn — ENET_W_Rn 27

ENET_RDYRTNn — ENET_RDYRTNn 27

ENET_CYCLEn — ENET_CYCLEn 27

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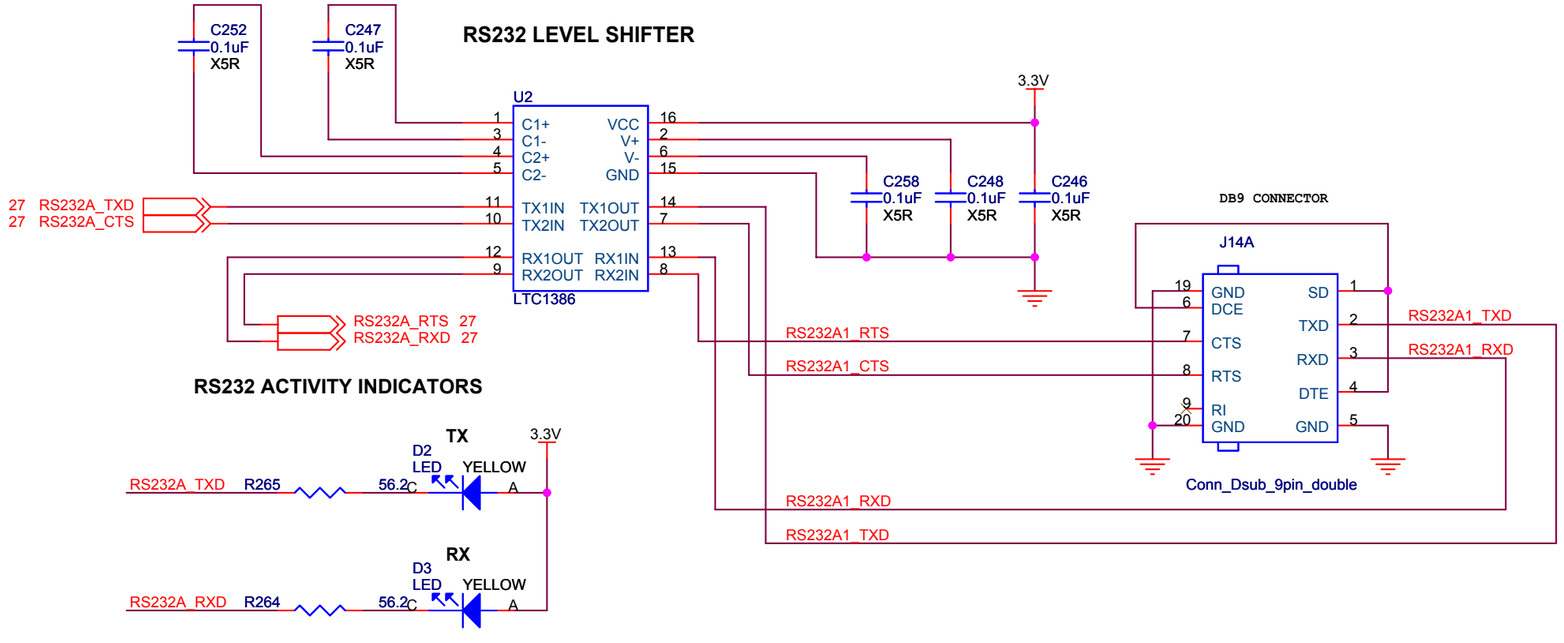
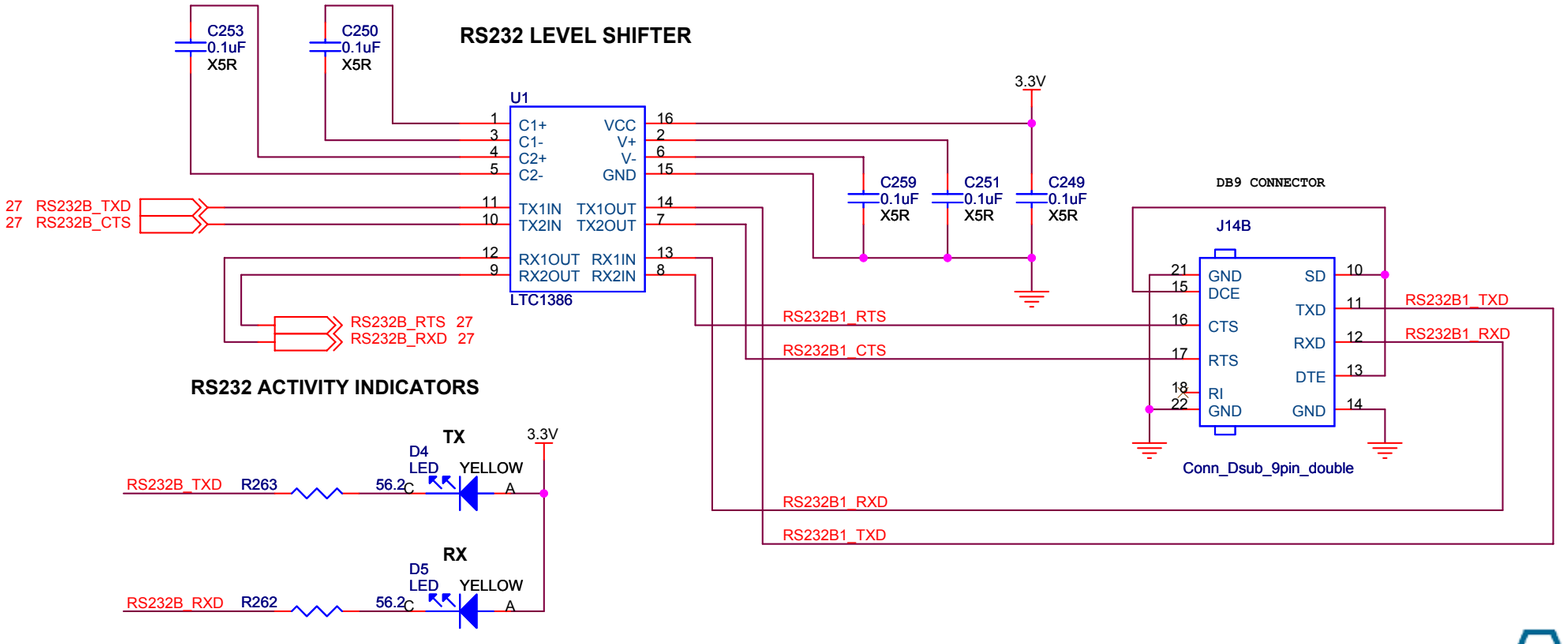
RS-232

PORT A



RS232 ACTIVITY INDICATORS

PORT B



RS232 ACTIVITY INDICATORS

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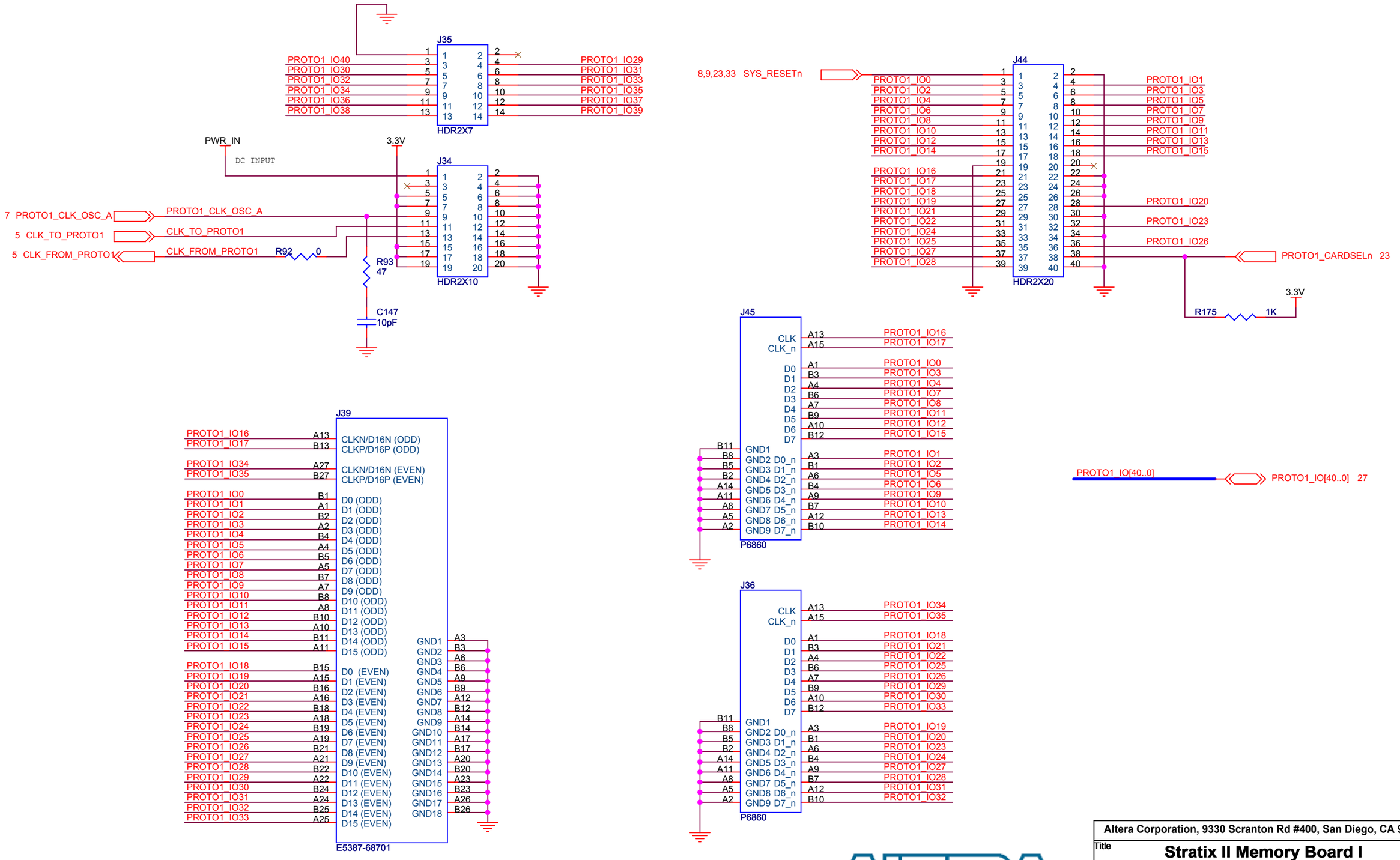
Debug Proto Headers



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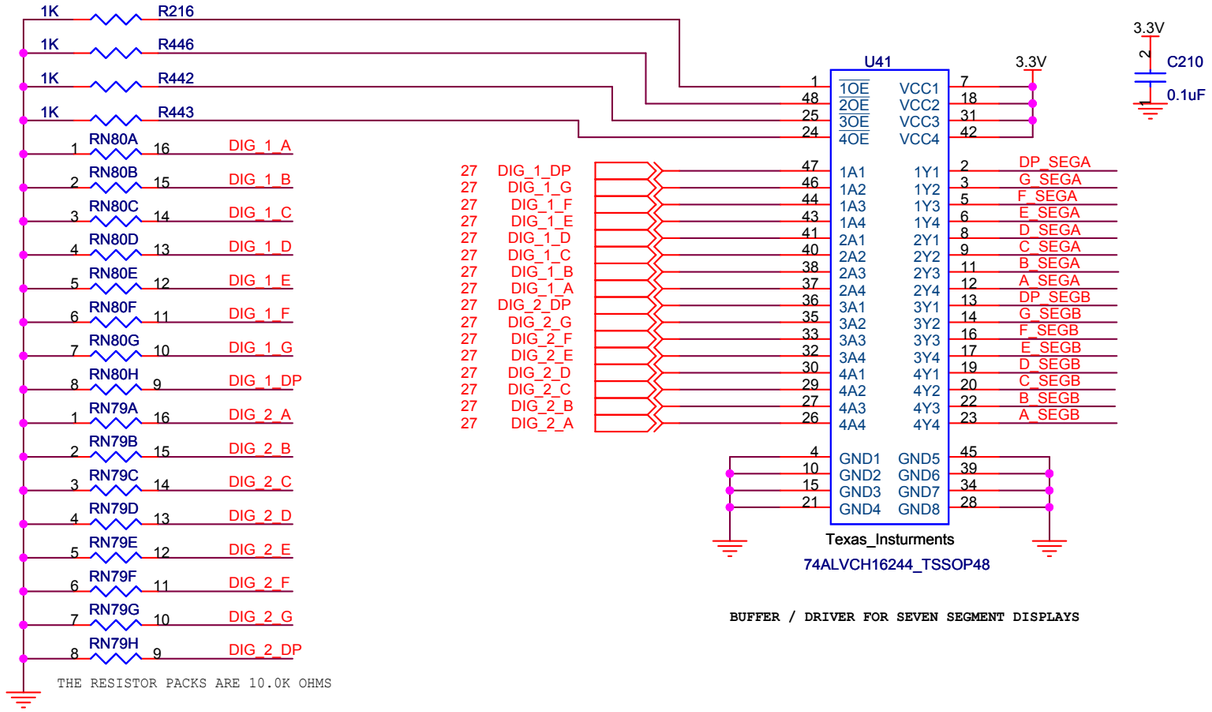
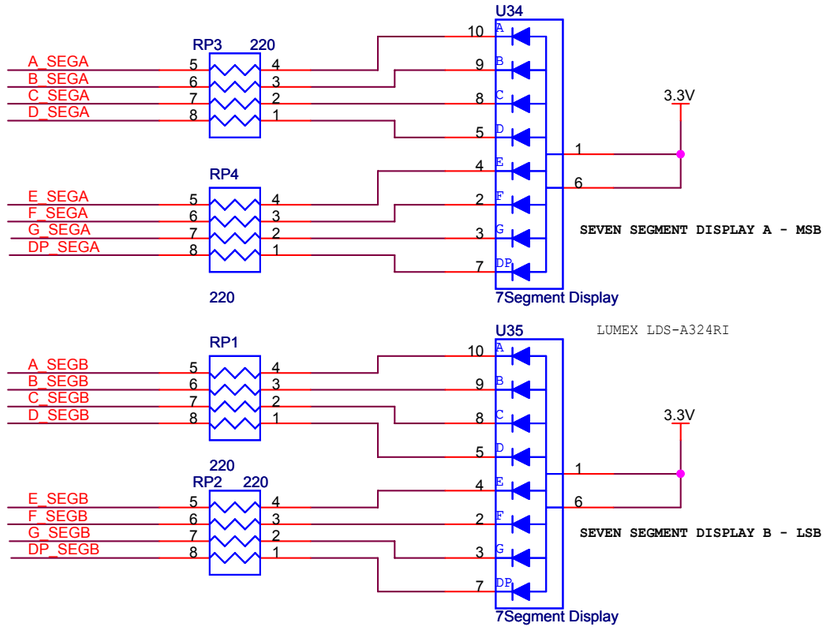
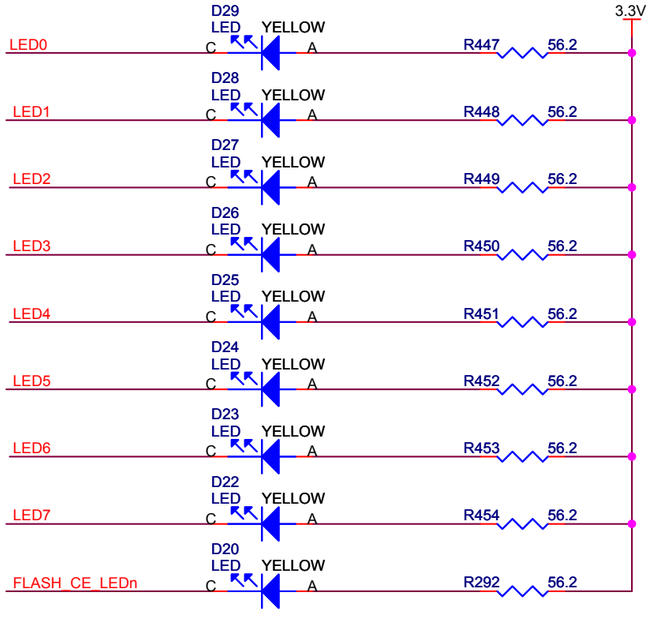
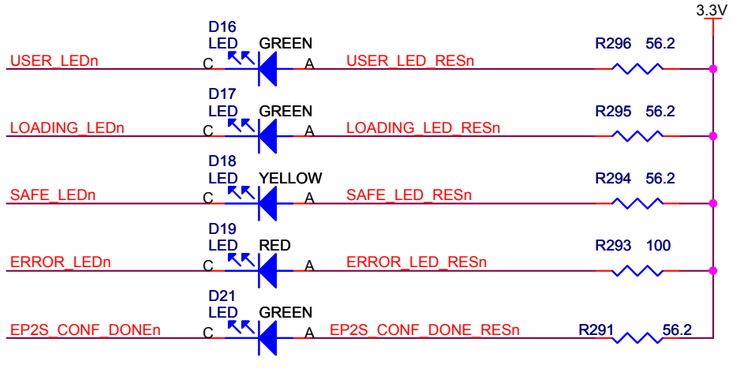
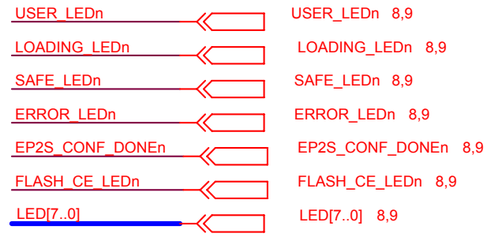
Seven Segment Displays & LEDs











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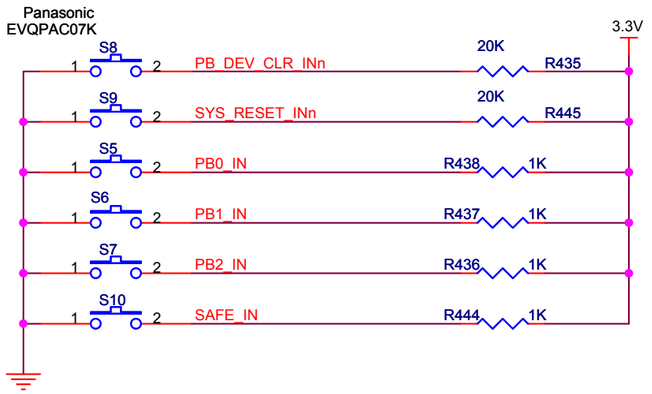
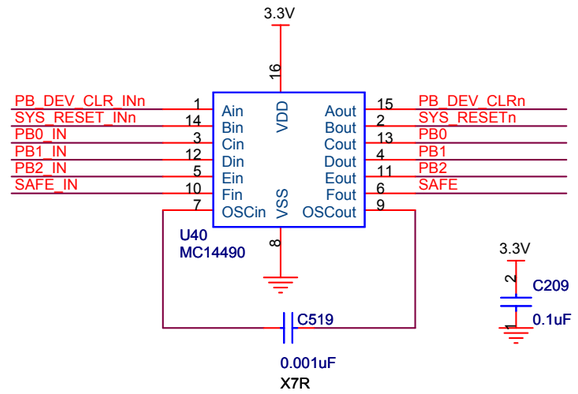
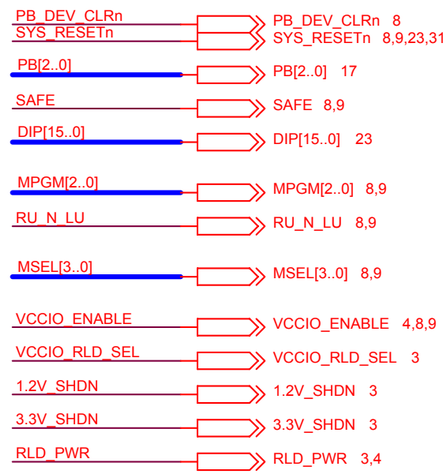
Push Buttons / Dip Switches

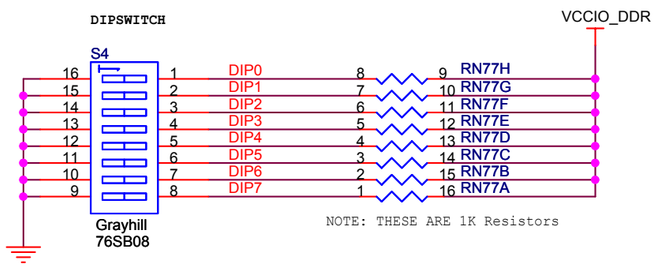
PUSHBUTTON SWITCHES







DIPSWITCH



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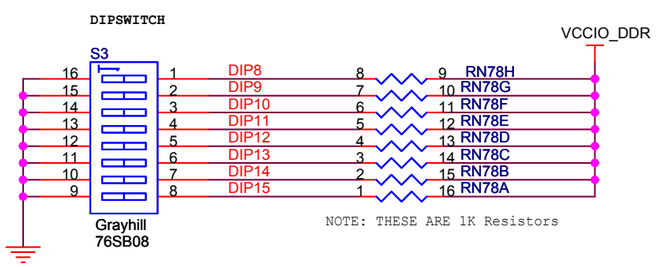

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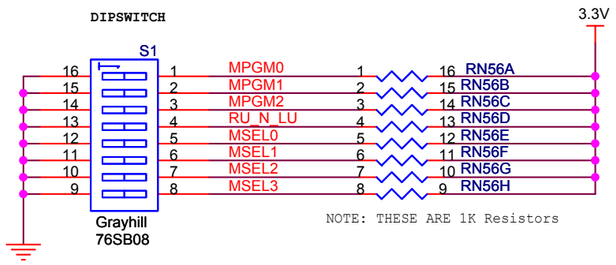
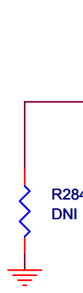


RLDRAM,1.5V



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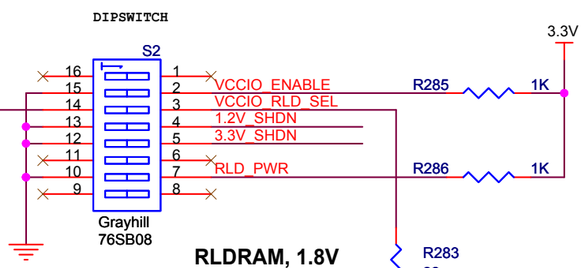
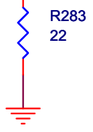


RLDRAM, 1.8V



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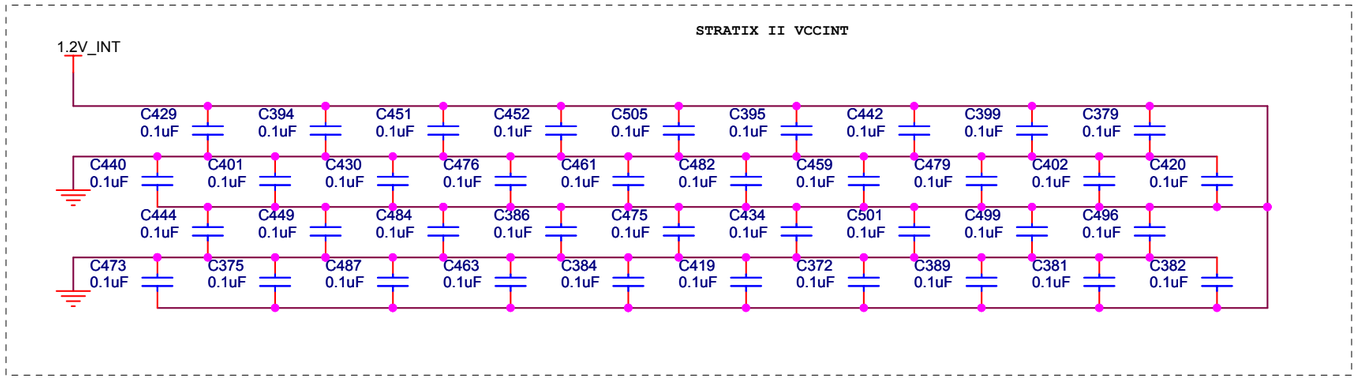
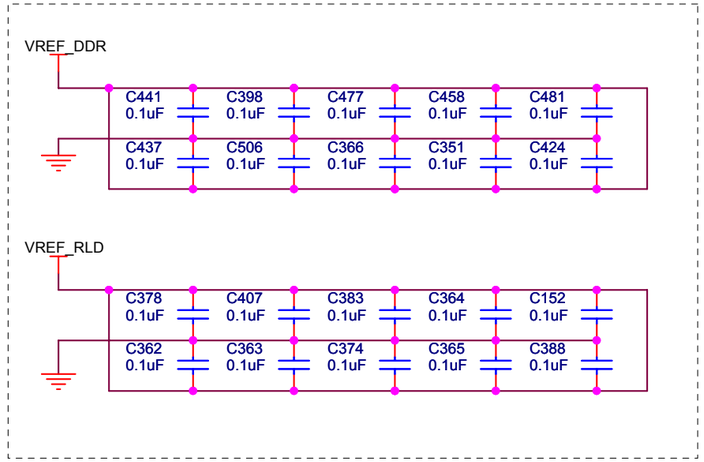
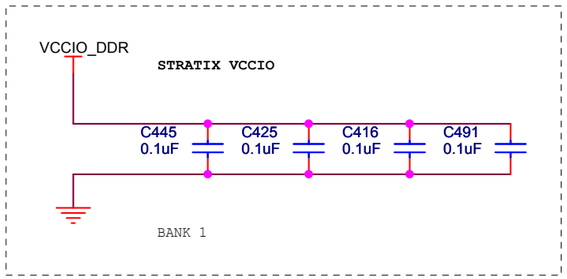
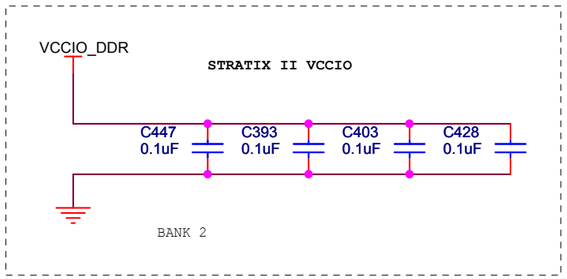
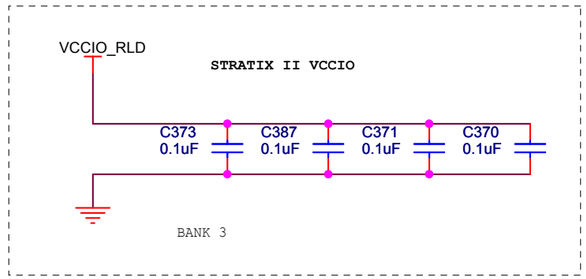
Stratix II Decoupling Capacitors

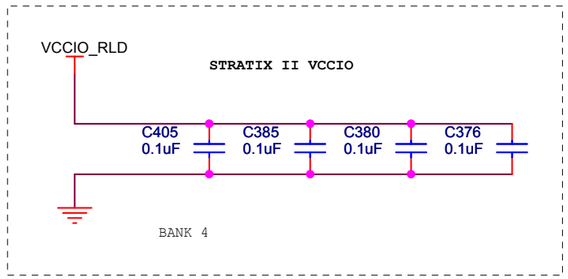


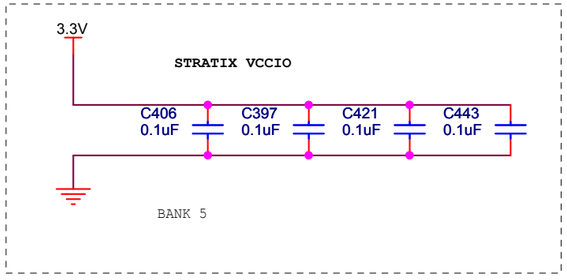


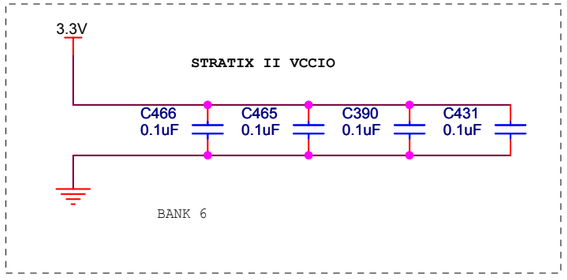


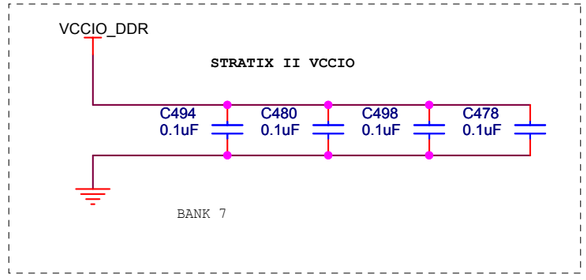


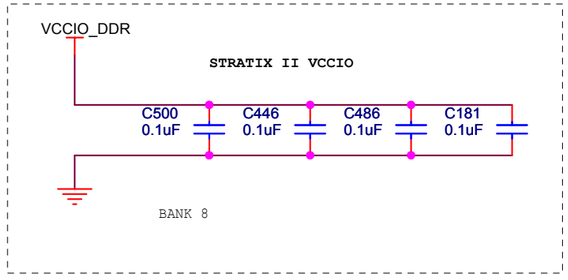


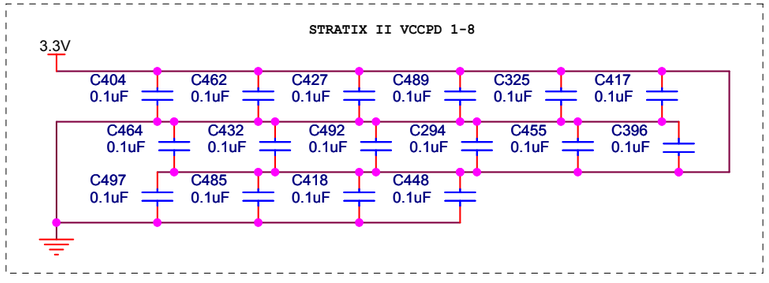


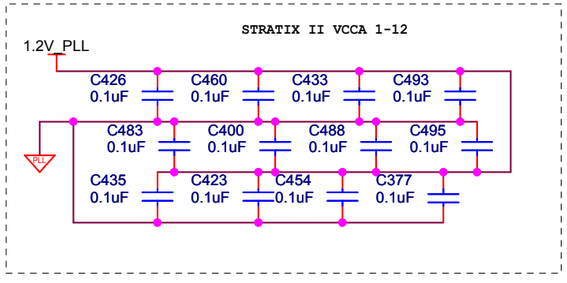


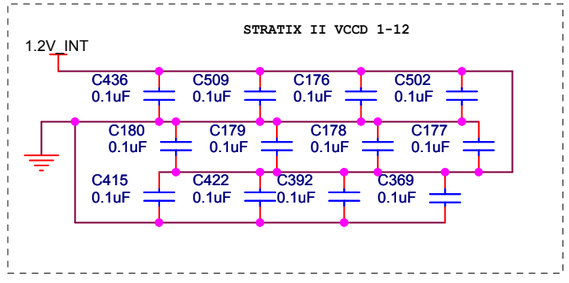












NOTE: PLACE ALL CAPACITORS ON THIS PAGE AS CLOSE AS POSSIBLE TO THE PINS OF THE STRATIX II DEVICE.

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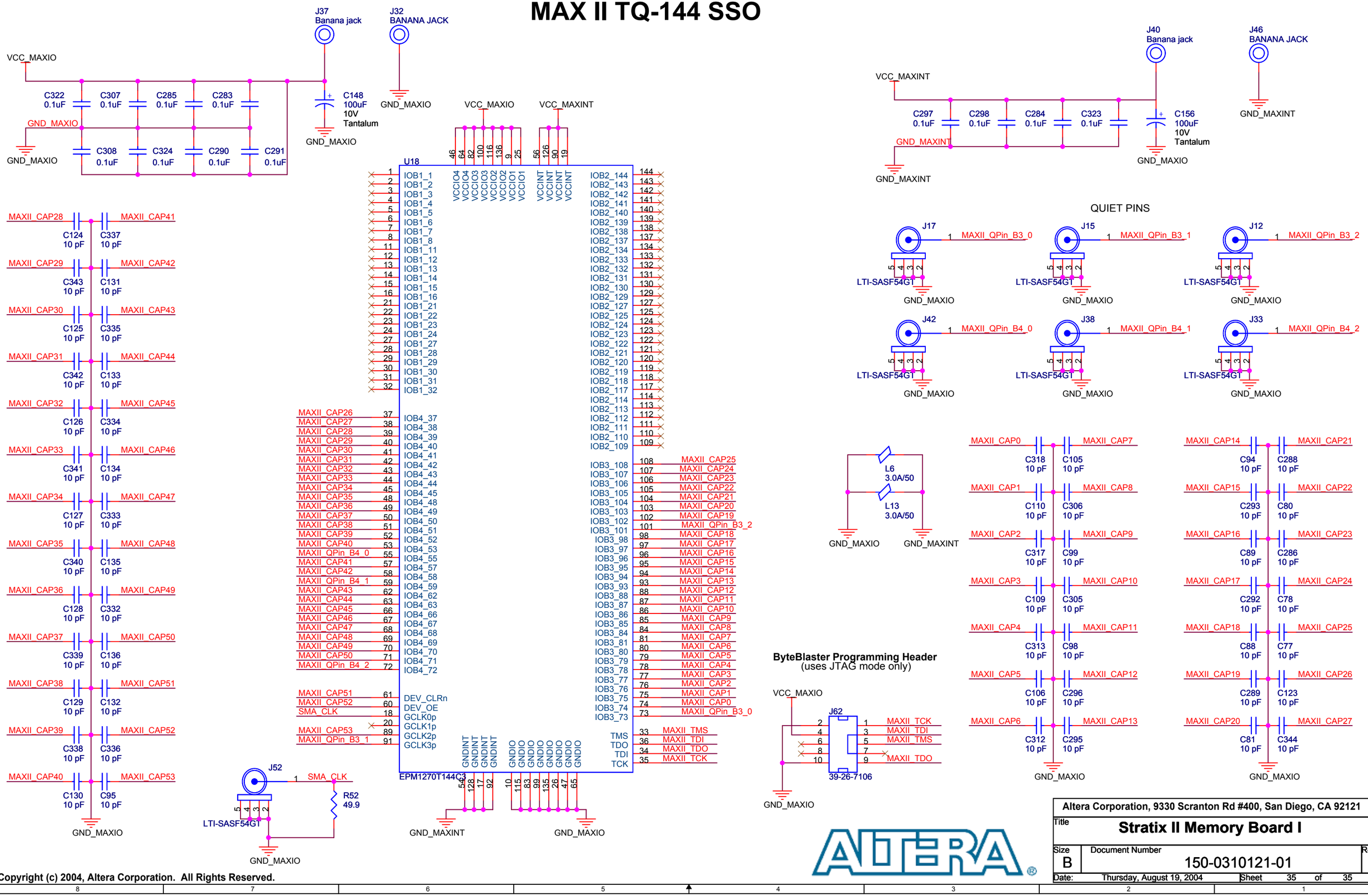
MAX II TQ-144 SSO



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